

A Hierarchical Control Scheme for Compensating Voltage Distortions in an Inverter Based Microgrid

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Nowadays increasing in nonlinear loads intensifies harmonic problems and voltage distortion in distribution systems. With appropriate control of Distributed Generation (DG) resources in a Micro Grid (MG), it is possible to enhance the MG power quality. This paper proposes a hierarchical control method for Inverter Based Distributed Generators (IBDGs) to compensating voltage distortions such as: voltage harmonics, voltage unbalance and voltage sag and swell in Sensitive Load Bus (SLB). This method consists of two control level of primary and secondary. The secondary control proposes a selective harmonic compensating method and voltage unbalance compensation appropriately according to DGs impact on harmonic resonances. Some buses have more participation in exciting of the MG resonance modes. Therefore, larger harmonic compensation factors are considered for the IBDGs that are near to these buses. For the other IBDGs, the voltage unbalance compensation factor is selected bigger. On this basis, the Participation Factor (PF) of buses in different resonances is identified by network modal impedance analysis then, the compensation share of DGs would be prioritized accordingly. The primary control level includes of voltage controller, current controller, virtual resistor and DGs load compensation block. Effectiveness of the proposed control scheme is demonstrated through simulation studies. © 2018 Journal of Energy Management and Technology

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1. INTRODUCTION

The proliferation of nonlinear loads and power electronic equipment has caused high penetration of harmonic pollution and voltage unbalance in electrical systems [1]. This might result malfunction or overheating devices and motors. Usually DGs connect to the electric network by a power-electronic converter. The inverter in output stage of the DG is able to control output power, voltage or current. However, recently some control approaches are proposed to control the inverter for compensation of power quality problems [2–7]. For example in [2], each DG unit of MG is controlled as a negative sequence conductance to compensate voltage unbalance. An autonomous voltage unbalance compensation scheme which works based on the local measurements is proposed in [3] for DGs of an islanded MG. In [4–7], the inverters emulate a resistance at harmonic frequencies to compensate voltage harmonic distortion. The discussed methods in [2–7] are designed for compensation of voltage unbalance or harmonics at each DG terminal while the power quality at the SLB is the main concern due to the sensitive loads [8]. Thus, a good power quality can be guaranteed for

the sensitive loads connected to SLB by compensation of SLB voltage harmonics and unbalance.

The concept of MG hierarchical control was applied for cooperative compensation of voltage unbalance [9, 10] and harmonics [11, 12] at the network SLB. In this regard, a two-level hierarchical control approach for IBDGs in MG applications was proposed in [13]. In this strategy the control structure comprises a virtual impedance loop that is set by the central controller to mitigate the voltage distortion at SLB. However, the unbalanced voltage drop across the virtual impedance is not considered, which leads to a limited performance for the unbalance compensation of the output voltage. On the other hand, in [14] an enhanced control structure was proposed for a MG in which the DGs are properly controlled to compensate voltage unbalance and harmonics to achieve a high voltage quality at the SLB. In most of the previous compensation methods, the IBDGs contribute in the compensation with the same priorities while the location of DGs has a significant effect on the compensation of voltage distortion.

In this paper a hierarchical control strategy is applied to com-

compensate the voltage harmonics and unbalance at SLB in a MG. The proposed hierarchical control scheme consists of two levels. The primary control comprises of local controllers in order to provide proper sharing of fundamental and non-fundamental powers among the IBDGs. In the secondary control, at the first resonance analysis is carried out for the MG using the modal impedance analysis and harmonics compensation priorities at different nodes are identified. Then, a selective compensation scheme is used for assigning the calculated harmonic and unbalance compensation priorities on IBDGs at different position for improved compensation performance. Then an effective virtual impedance method [15], is used in IBDGs control system for the damping of distortions.

The rest of the paper is organized as follows. In section 2, the network modal impedance analysis is discussed. In section 3, compensation of voltage distortion by proposed control scheme is investigated. In section 4, compensation priority coefficients of MG are identified. Simulation of case study is carried out in section 5, and finally the conclusions are presented in section 6.

2. CONCEPT OF RESONANCE MODES

The frequency scan method in order to detect the system resonances was implemented in [16]. But this method cannot identify the component and bus that excites the resonance. To solve this problem, the modal impedance analysis was used in order to identify system resonances [17]. In this method at first, the system admittance matrix is acquired. Then, modal impedance matrix $[Z_m]$, is calculated by using of Eqs. (1) to (3). According to these equations, if input current vector $[I]$ is always set to 1 p.u., so the high voltage vector $[V]$ values are associated with the singularity of the admittance matrix $[Y]$. This singularity of $[Y]$ matrix can be found when one of its eigenvalue is close to zero.

$$[V] = [Y]^{-1} \cdot [I] \quad (1)$$

$$[V] = [L] [\Lambda]^{-1} [T] \cdot [I] \quad (2)$$

$$[Z_m] = [\Lambda]^{-1} \quad (3)$$

where $[T]$, $[L]$ and $[\Lambda]$ are matrices that constructed from right eigenvectors, left eigenvectors and diagonal matrix composed of eigenvalues of the MG admittance matrix, respectively. Clearly, if the eigenvalues of $[\lambda]$ matrix tend to smaller amounts, the modal impedances of $[Z_m]$ matrix move towards the big values and cause the propagation of parallel resonances. The critical modal impedance (highest modal impedance) is much higher than other modal impedances. In the presence of the critical mode (for example mode number 1), the matrix $[Z_m]$ can be estimated as follows and the Participation Factor (PF) matrix is also obtained afterwards:

$$\begin{bmatrix} Z_{m,1} & \dots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \dots & Z_{m,n} \end{bmatrix} \approx \begin{bmatrix} Z_{m,1} & \dots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \dots & 0 \end{bmatrix} \quad (4)$$

PF

$$[V] = Z_{m,1} \cdot \begin{bmatrix} L_{11} \cdot T_{11} & \dots & L_{1n} \cdot T_{1n} \\ \vdots & \ddots & \vdots \\ L_{n1} \cdot T_{n1} & \dots & L_{nn} \cdot T_{nn} \end{bmatrix} \cdot [I] \quad (5)$$

The PF matrix represents the impact of each bus on the critical modes. In this matrix, the number of rows matches with node number and the number of columns represents the number of impedance modes. Also, $Z_{m,i}$ represents the impact factor (weight) of modes at different harmonic frequencies. Since modal impedances for different modes can be compared, using $Z_{m,i}$ as a weighting factor will make the mode comparison of participation factors possible. In order to obtain the appropriate weight, the maximum point of each mode is normalized according to the highest magnitude mode.

3. MG HIERARCHICAL CONTROL SCHEME

Fig. 1 presents the proposed hierarchical plan for compensating harmonics and voltage unbalance at SLB in a MG. The MG includes of many voltage control and current control IBDGs which are connected to SLB via distribution lines. Furthermore, many nonlinear and unbalance loads are also considered in this bus. The hierarchical control plan consists of two levels of primary and secondary level, where the secondary control should collect the required data from SLB and produce appropriate reference control signal for IBDGs. As seen, SLB voltage harmonics data are extracted by the measurement block and sent to IBDGs with Low Bandwidth Communication (LBC). In order to ensure that LBC is sufficient, the transmitted data should consist of approximately dc signals. Hence, the SLB voltage harmonic components are in dq (synchronous) reference frame. In local controllers, these signals are returned to $\alpha\beta$ (stationary) reference frame for compensation. Detail of primary and secondary control plan is presented in the following.

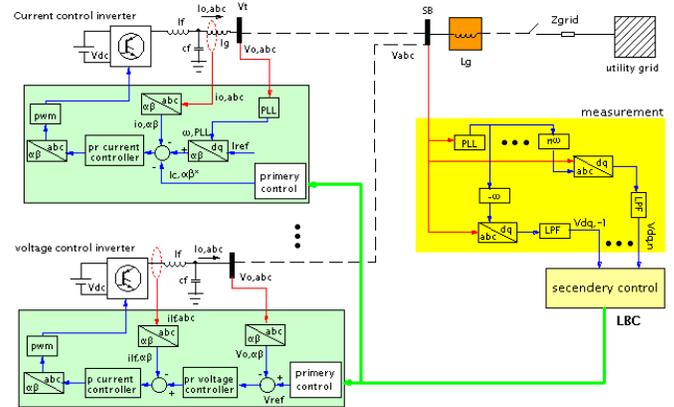


Fig. 1. Control structure and power section of hierarchical control plan.

A. Secondary Control Level

Block diagram of secondary control level is presented in Fig. 2. To establish voltage and frequency in desired amount in the SLB, voltage and frequency errors are set using PI controllers and the output signals are sent to primary control of voltage control resources. As it is clear, ω_{ref} and E_{ref} are frequency and voltage reference in SLB and are usually set to 1 p.u. The main component voltage and frequency signals are sent to primary control level of i th bus, after multiplying at frequency index and voltage magnitude index ($E I_i$ and ωI_i). These two coefficients are only used for control voltage resources and the compensation share of resources can be configured by these factors. Also, $E I_i$

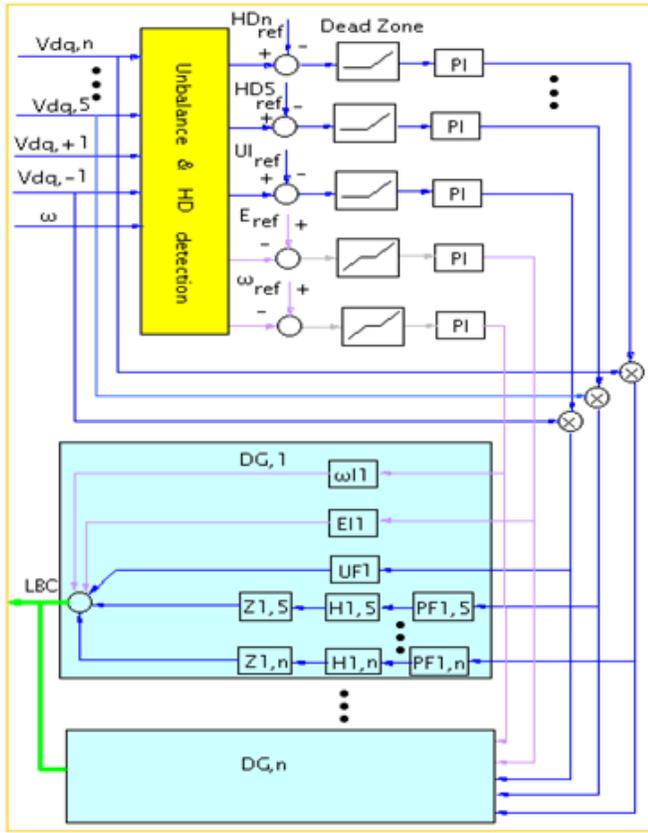


Fig. 2. Control details of secondary level.

and ωI_i are zero for control current resources. The dead zone block for frequency and voltage magnitude signals prevents of controller to operation in a limited band near reference value in order to avoid of boundary oscillations.

To maintain voltage quality of SLB, the amount of permissible voltage unbalance and magnitude of low order harmonics in this bus are identified as reference signals for compensation. Afterward, the voltage Unbalance Index (UI) and Harmonic Distortion (HD) of SLB are compared with the associated reference values (UI_{ref} and $HD_{i,ref}$), acquired errors are sent to PI controllers. Then the output signals are multiplied by $V_{dq,i}$ to create compensation reference signals. The dead zone block is considered for voltage harmonics and unbalance to prevent operation of PI controller in case that the produced error was less than the amount of reference signal. The DGs compensation priority is identified by arrays of participation factor matrix, magnitude of the critical impedance and load harmonics. The $PF_{i,j}$ represents the participation of i th bus according to its situation in compensating j th harmonic. Modal impedance factor $Z_{i,j}$ indicates the effect of i th critical mode in j th harmonic. Load harmonic factor $H_{i,j}$ is identified by the j^{th} harmonic order of load current in i^{th} bus.

The unbalance compensation factor of UF_i represents the share of i th DG in compensating the voltage unbalance. Some buses have more participation in exciting of the MG resonance modes. Therefore, larger harmonic compensation factors are considered for the IBDGs that are near to these buses. For the other IBDGs, the voltage unbalance compensation factor UF_i is selected bigger.

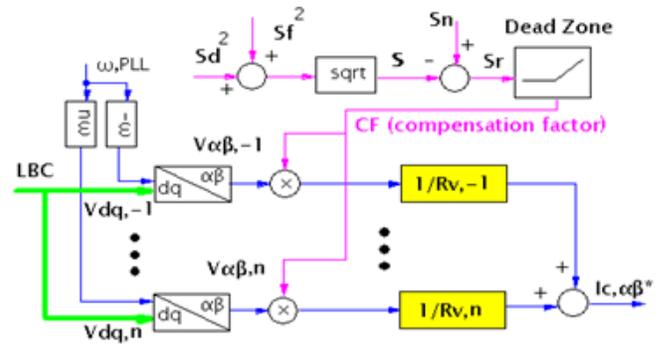


Fig. 3. Local control of current control resources.

B. Primary Control Level

B.1. Local control of current control resources

The detail of primary level of current control DG has been presented in Fig. 3. The received signals from secondary control level after returning to β stationary frame, are sent to the DG load compensation block. This block configures the compensation share of each IBDG according to its extra capacity. As shown in this block S_n, S_f, S_d, S and S_r are nominal power of IBDG, positive sequence output power, distortion output power, total output power and free capacity of IBDG, respectively. According to standard [18], produced distortion power of each inverter can be calculated as follows:

$$S_d = S_f \cdot \sqrt{THD_I^2 + THD_V^2} \quad (6)$$

where, THD_I and THD_V are current and voltage total harmonic distortions. Afterwards, S_r can be calculated as shown in figure according to nominal power S_n and total output power S . The output signal of dead zone block of this figure can be presented as follows:

$$V_{\alpha\beta,j} = \begin{cases} V_{\alpha\beta,j} (S_n - \sqrt{S_d^2 + S_f^2}) & S_r > 0 \\ 0 & S_r < 0 \end{cases} \quad (7)$$

where, j represents harmonic order. According to the Eq. (7), if $S_r < 0$, with increasing in the total output power S , S_r reduces which represents reduction of IBDG load. In other word, there is a inherit negative feedback in this equation which divides the compensation load between the IBDGs appropriately. Also, if S_r is less than zero, dead zone block prevents of any attempt for compensation to avoid of DGs overload. The produced negative sequence component and voltage harmonic signals are sent to the virtual damping resistor block to multiply signals by $1/R_{v,i}$. Afterwards, the compensation reference of each harmonic is generated separately and then, all of the compensation references are added together. Finally, total compensation reference $I_{c,\alpha\beta}^*$ is inserted as a current reference in the control system, as shown in Fig. 1.

B.2. Local control of voltage control resources

Detail of primary control level of voltage control DGs is presented in Fig. 4. According to Fig. 4, signals associated with frequency and voltage magnitude are added to resources droop characteristic block and cause retrieval SLB voltage and frequency.

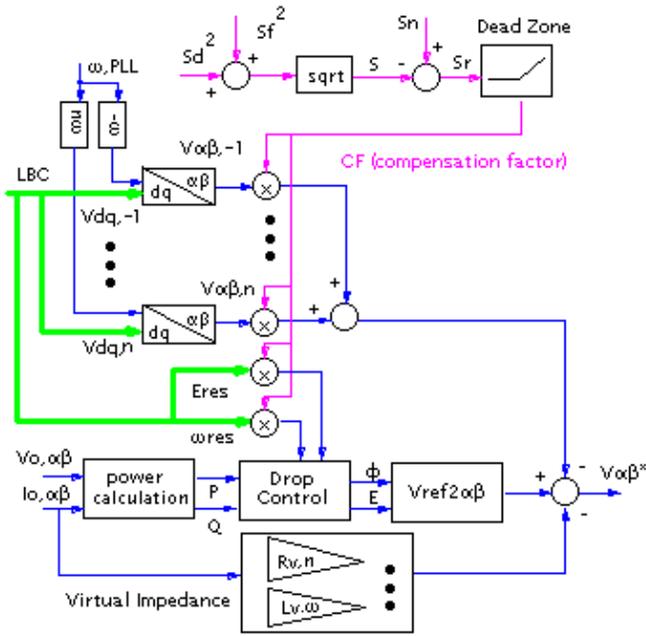


Fig. 4. Local control of control voltage resources.

$$\varphi^* = \varphi_0 + \int \omega_{ress} + (K_{pp} + \frac{K_{iv}}{s})(P^* - P) \quad (8)$$

$$E^* = E_0 + E_{res} + K_{PQ}Q.(Q^* - Q) \quad (9)$$

These equations represent the resources drop characteristic, in which ω_{ress} and E_{res} are reference frequency and voltage that are sent from the secondary control level to the local control of resources, also φ_0 is the load angle (the angle between E and V) and E_0 is the desired voltage magnitude. The parameters of K_{PP} , K_{ip} , K_{PQ} , φ^* , E^* , P^* , and Q^* are proportional coefficient of active power, integral coefficient of active power, proportional coefficient of reactive power, reference of load angle, reference of voltage, reference of active power and reference of reactive power, respectively. The virtual impedance block is assumed for basic frequency as L_v inductance in order to improve power sharing among resources, and in harmonic components it is assumed as $R_{v,n}$ resistor for providing damping in voltage harmonics.

Voltage control resources can participate in adjusting the MG voltage by injecting reactive power. The amount of this compensation share can be adjusted by setting of resources drop characteristic K_{PQ} factor). Generally, the compensating of main component voltage in MG is difficult due to low impedance of upstream network since it requires injecting high amount of current. Therefore, the inductance L_g is added to the network [20]. In this situation, according to Fig. 5 for single inverter case, it can be seen:

$$\vec{I}_c = \vec{I}_G + \vec{I}_L \quad (10)$$

where I_C , I_G and I_L are the currents of inverter, grid and load, respectively. First, it is assumed that transferred power of inverter to grid is active power. In normal situation, magnitude of E and V are almost equal, inverter supplies power to load and extra active power flows through L_g into the network. In this case, the network current is real component $\vec{I}_G = I_{Gd}$. Fig. 6.a represents vector diagram of network currents and voltages.

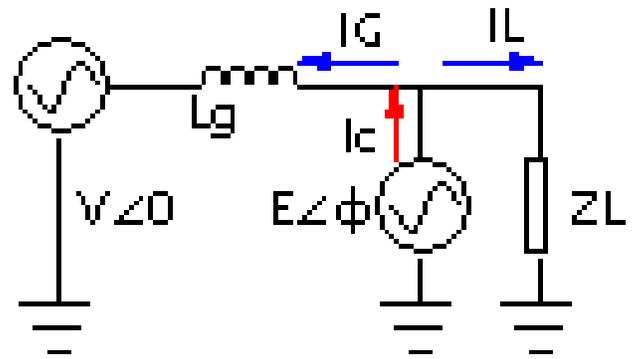


Fig. 5. Connected inverter to infinite bus via L_g inductance.

To compensate the decrease or increase of the main component voltage during voltage changes, inverter controllers should be designed so that it can supply required reactive power during voltage change.

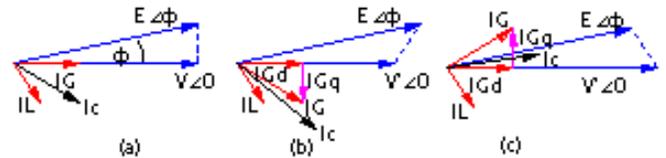


Fig. 6. a) Network voltages and currents before reduction of network voltage. b) Network voltages and currents after reduction of network voltage. c) Network voltages and currents after increasing network voltage.

For example when the network voltage drop $V' < E$, the inverter in addition to supplying load and network, should inject reactive power in order to adjust load voltage (Fig. 6.b). In this situation, imaginary component of I_{Gq} is added to network current (equation (11))

$$\vec{I}_G = I_{Gd} + jI_{Gq} \quad (11)$$

$$\vec{I}_G = \frac{E\angle\varphi - V\angle 0}{jx} \quad (12)$$

According to equation (12), it can be observed that during voltage changes, the amount of injecting current for adjusting the voltage is proportional with inverse of network impedance. This means that high impedance reduces the changes. In the proposed topology DG is connected to the network via L_g inductance. According to limitation of power transmission and line impedance equation:

$$X < \frac{E}{P_{max}} \quad (13)$$

It can be concluded from equation (13) that maximum transmission power limits the inductance. In this structure voltage is controlled with adjusting reactive power and independent from frequency. However L_g impedance cannot be selected too high since the voltage regulation is effected directly [20].

4. THE MG MODEL AND MODAL ANALYSIS

Fig. 7 represents the single line diagram of a three-phase balanced MG. The implemented inverters are current control and voltage control types. In the following section, the inverter control equations and MG equivalent circuit are acquired.

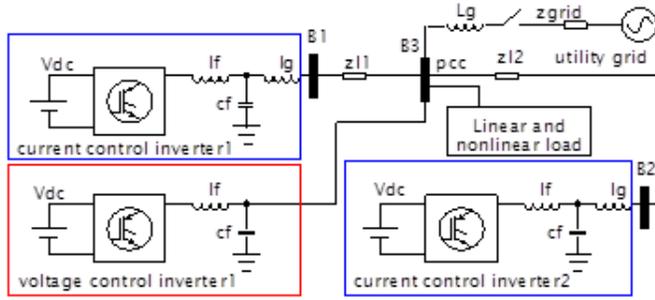


Fig. 7. Single line diagram of the MG.

A. Current Control Inverter Model

Fig. 1 represents block diagram of current control inverter. As it can be seen, the inverter output voltage is synchronized with MG voltage by a Phase Locked Loop (PLL). In the inverter output is LCL filter and inverter control loop includes PR controller in stationary reference [19]. The inverter control system can linearized around its operation point [21] and its transfer function can be acquired as follows:

$$I_0(S) = G_{cc}(S) \cdot I_{ref}(s) - Y_{oc}(S) \cdot V_0(s) \quad (14)$$

Equation (14) represents the Norton equivalent circuit of current source inverter, where $G_{cc}(S)$, $Y_{oc}(S)$, I_{ref} and $V_0(s)$ are closed loop transfer function, output admittance, reference current and inverter output voltage, respectively. G_{cc} and Y_{oc} are acquired according to the control system as follows:

$$G_{VV}(s) = \frac{G_V(S) \cdot G_I(s) \cdot G_{pwm}(S)}{C_f \cdot s \left((s \cdot L_f) + G_I(s) \cdot G_{pwm}(S) \right) + G_V(S) \cdot G_I(s) \cdot G_{pwm}(S) + 1} \quad (15)$$

$$Y_{oc}(S) = \frac{(C_f \cdot s)(s \cdot L_f) + 1}{(C_f \cdot s)(s \cdot L_f)(s \cdot L_g) + (s \cdot L_f) + (s \cdot L_g) + G_I(s) \cdot G_{pwm}(S)} \quad (16)$$

where G_I , G_{pwm} , L_f , L_g and C_f are transfer function of proportional controller, transfer function of the inverter, inverter side inductance, grid side inductance and filter capacitor. G_I and G_{pwm} are defined as follows:

$$G_I(s) = K_{pi}I + \sum_{K=1,5,\dots,19} \frac{K_{ri} \cdot s}{s^2 + (k \cdot \omega_0)^2} \quad (17)$$

$$G_{pwm}(s) = \frac{1}{1 + 1.5 \cdot T_s \cdot s} \quad (18)$$

where K_{ri} , ω_0 , K_{pi} and T_s are resonance coefficient, basic frequency, proportional factor and switching period.

B. Voltage Control Inverter Model

The detail of voltage control inverter has been shown in Fig. 1. Voltage control inverter has an LC output filter and control is carried out in stationary reference frame. The internal control loop consists of P controller and external loop consists of PR

controller. The control system can be linearized around its operation point and input output relation can be acquired based on the inverter transfer function and output impedance according to the following equation [21].

$$V_0(S) = G_{vv}(S) \cdot v_{ref}(s) - Z_{ov}(S) \cdot i_0(s) \quad (19)$$

Equation (19) represents the Norton equation circuit of the voltage source inverter where $G_{vv}(S)$ and $Z_{ov}(S)$ are closed loop transfer function and inverter output impedance.

$$G_{VV}(s) = \frac{G_V(S) \cdot G_I(s) \cdot G_{pwm}(S)}{C_f \cdot s \left((s \cdot L_f) + G_I(s) \cdot G_{pwm}(S) \right) + G_V(S) \cdot G_I(s) \cdot G_{pwm}(S) + 1} \quad (20)$$

$$Z_{ov}(S) = \frac{L_f \cdot s + r_f + G_I(S)}{C_f \cdot s \left((s \cdot L_f) + G_I(s) \cdot G_{pwm}(S) \right) + G_V(S) \cdot G_I(s) \cdot G_{pwm}(S) + 1} \quad (21)$$

where, $G_v(s)$ and $G_I(s)$ are external loop (voltage loop) transfer function and internal loop (current loop) transfer function which are defined as follows:

$$G_v(s) = K_{pv}V + \frac{K_{rv} \cdot s}{s^2 + (\omega_0)^2} \quad (22)$$

$$G_I(s) = K_p I \quad (23)$$

where K_{rv} , K_{pv} and K_p are voltage resonance coefficient, voltage proportional coefficient and current proportional coefficient.

C. Identification of the Priority Factors

In the first, the admittance matrix is constructed for the MG in Fig. 7. It is assumed that the MG is disconnected to the upstream grid and the voltage control inverter is in service. In order to more precision in the identifying of system resonances, the output impedance of IBDGs is considered in the MG admittance matrix.

$$\begin{bmatrix} Y_{oc,1} + Y_{l,1} & 0 & -Y_{l,1} \\ 0 & Y_{oc,2} + Y_{l,2} & -Y_{l,2} \\ -Y_{l,1} & -Y_{l,2} & Y_{ov} + Y_{load,pcc} + Y_{l,1} + Y_{l,2} \end{bmatrix} \quad (24)$$

where $Y_{l,i}$ and $Y_{load,pcc}$ are line and load impedances. Y_{ov} and $Y_{oc,i}$ are also output admittance of voltage control inverter and current inverter. The modal analysis is carried out for the MG of Fig. 7 to identify the participation factors of the buses. By considering the parameters of control system and power circuit listed in Table 3, the MG resonances will be studied. At first, in order to identify the effect of inverters output impedance in the creating of resonances, the MG modal impedance analysis is carried out without considering the output impedance of inverters. Regardless of the output impedances, the MG is same as of the inductance network, therefore no resonance is observed in the system (Fig. 8).

Considering the effect of inverters output impedance, due to existence of capacitor in the inverters output filter, as it is cleared in Fig. 9 the magnitude of modal impedances have critical values in the low order frequencies. According to Table 1 and Fig. 9, the maximum points in low order frequencies are related with the third and second modes which are occurred at 11.2th and 13.7th harmonic orders, respectively. Bus 2 and bus 1 have the highest participation factor of creating these resonance modes.

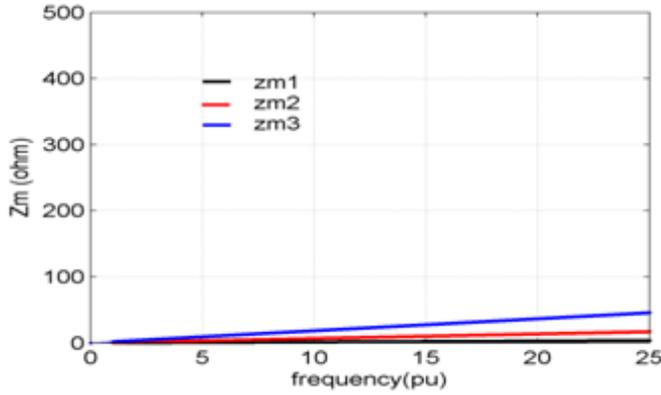


Fig. 8. The magnitude of network impedance modes.

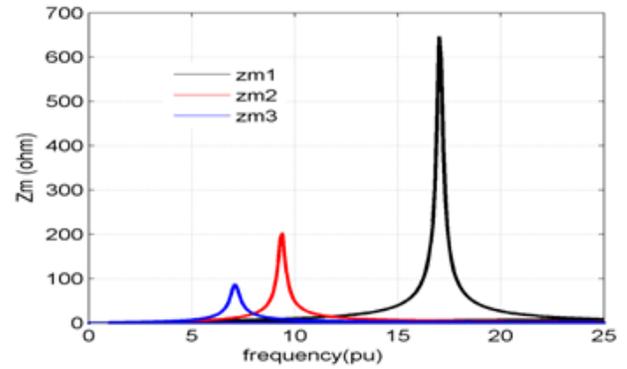


Fig. 10. MG impedance modes with five inverters.

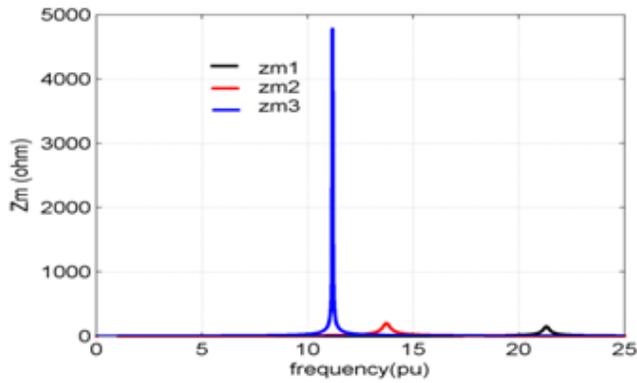


Fig. 9. Network impedance modes considering the effect of resources output impedance.

Table 2. MG participation factors with five inverters.

Harmonic order	Critical impedance Z_{ij}	Participation factor PF_{ij} of:		
		Bus1	Bus2	Bus3
7.18	87.8	0.29	0.51	0.62
9.07	206.82	0.45	0.49	0.25
17.13	658.85	0.33	0.04	0.86

the modal impedance analysis, creates inaccuracy in the identifying of buses participation factors and the lines current quality can be severely distorted.

Therefore, the 11th harmonic at bus 2 and 13th harmonic at bus 1 need to the more attenuation, and the compensation share of these two buses should be more than other IBDGs for these harmonics.

5. SIMULATION RESULTS

The MG resonances can be excited by the main grid. The resonance frequencies are also affected by the number of parallel inverters. Further considering that the main grid voltage often contains some low order steady state harmonics, significant steady state harmonic currents can be produced due to the effects of resonances. For example, when the MG is connected to the upstream grid and five current control inverters with the same specifications are included in the MG, one of the resonance frequencies is around 350 Hz, which may excite the seventh steady state resonance in a 50 Hz system (Fig. 10 and Table 2).

In order to prove the efficiency of the proposed method, simulation is carried out for The MG of Fig. 7 in network connected and island situations. The nonlinear load of bus 3 is a three phase rectifier with 200Ω load and 220F capacitor. In addition in order to create unbalance, a single phase load is placed between phases A and B. the compensation is carried out first in uniform method (all DGs participate in compensation with the same priority) and then in non-uniform method (the DGs participate in compensation with the different priority) and results are presented in Fig. 11. It is assumed that current control inverters are able to supply all the loads in the Point of Common Coupling (PCC), and the capacity of voltage source is used in order to transmit power to upper network.

Due to the impacts of the aforementioned resonances, it can be concluded that neglecting the inverters output impedance in

The simulation is carried out in seven steps: The first step ($0 \leq t < 0.4s$): in this step, linear, nonlinear and unbalance loads are connected to the PCC bus. The simulation is started with zero initial values for resources and after the initial transient situation, it goes to stable state. Current reference of inverter 1 is set to 15 A and inverter 2 is set to 25 A, and the power reference of inverter 3 is set to $P^*=10KW$ and $Q=0Var$. The MG sends almost 10KW of power to upstream network and no compensation is carried out. The effective voltages and powers in bus 3 and grid line are shown in Figs. 11.a and 11.b.

Table 1. Critical impedance and participation factor.

Harmonic order	Critical impedance Z_{ij}	Participation factor PF_{ij} of:		
		Bus1	Bus2	Bus3
11.21	478	0.25	0.59	0.14
13.74	21.13	0.57	0.37	0.05
21.32	15.13	0.16	0.02	0.80

Step two ($0.4s \leq t < 0.9s$): in this step, compensation blocks are activated and DGs participate in compensating harmonics and voltage unbalance with the same priority. The voltage THD and voltage negative sequence at bus 3 in compensated state are reduced to 9

Step three ($0.9s \leq t < 1.4s$): in this step non-uniform com-

Table 3. Parameters of the power and control system.

Symbol	Parameter	Value	Unit
E	Grid voltage amplitude	311	V
V_{dc}	DC link voltage	650	V
ω_0	Grid frequency	314	Rad/s
$Z_{load,pcc}$	Load impedance	10	Ω
Z_{UL}	Unbalance load	20	Ω
L_g, L_{1f}	filter Inductance 1	0.2,1.8	mH
L_{2f}	filter Inductance 2	1.8	mH
F_s	Switching frequency	10	KHz
Z_{l1}, Z_{l2}, Z_{grid}	Line Inductance	$j0.72, j0.42, j0.2$	Ω
L_g	Interconnection Inductance	11	mH
$R_{v,-1}, R_{v,5}, R_{v,7}, R_{v,11}, R_{v,13}$	virtual resistance1	9	Ω
$L_v / R_{v,5}, R_{v,7}, R_{v,11}, R_{v,13}$	virtual impedance2	1/2	mH/ Ω
C_f	filter Capacitor	25	μF
k_p, k_i^*	PI controller coefficient	.2,6	W/Rd
k_{p1}, k_{i1}^*	Resonance controller coefficient 1	1,100	W/Rd
$k_{p2}, k_{i2}^* / k_{p1}^*$	controller coefficient 2	.5,400/7	W/Rd
$K_{pp}, K_{ip} / K_{pi}^*$	Droop control	.00001, .0001 / .00005	W/Rd
H_{ij}^*	load harmonic factor	1	-
UF_1, UF_2, UF_3	unbalance factor	.5, .5, 1	-
ω_{I3}, EI_3	Voltage & frequency index	1, 1	-

pendation is activated at $t=0.9s$. In this case, the influence of IBDGs output impedance and the coefficients of participation matrix are considered in the compensation. The normalized values of Table 1 are used to assign DGs participation factors. In the non-uniform compensation method, the voltage THD is reduced to 4

Step four ($1.4s \leq t < 1.9s$): in this step a 0.15 p.u. reduction is occurred in the network voltage magnitude and the control voltage inverter can preserve MG voltage with injecting of 4KVar reactive power.

Step five ($1.9s \leq t < 2.4s$): in this step the network voltage is returned to normal situation again. The waveforms of inverters output currents, load power and SLB voltage are shown in Figs. 11.f to 11.j.

Step six ($2.4s \leq t < 2.9s$): in this step a 0.25 p.u. reduction occurs in the network voltage magnitude and the control voltage inverter supplies MG voltage with injecting a 7KVar reactive power. But since this amount of power is more than the inverter capacity (inverter capacity is assumed to be 12 KVA), the MG is separated from the network in 2.9 S and voltage control inverter supplies MG voltage and frequency independently.

Step seven ($2.9s \leq t < 3.4s$): in this step, the reactive power of voltage control inverter is reduced to 1KVar in order to adjust the MG voltage and its active power reduces to zero and MG operates in islanded mode. The THD waveform and voltage harmonics show that voltage distortion compensation is carried out properly in the islanded mode.

6. CONCLUSIONS

In this paper a hierarchical compensation method for improving the voltage quality of SLB in a MG is presented. The compensation method is non-uniform and compensation priorities for different DGs location and harmonic frequencies are identified for improved compensation performance compared to traditional compensation method. The priority factors are identified by modal impedance analysis of the MG. The control method consists of two primary and secondary control levels. In the secondary control level with assigning such compensation prior-

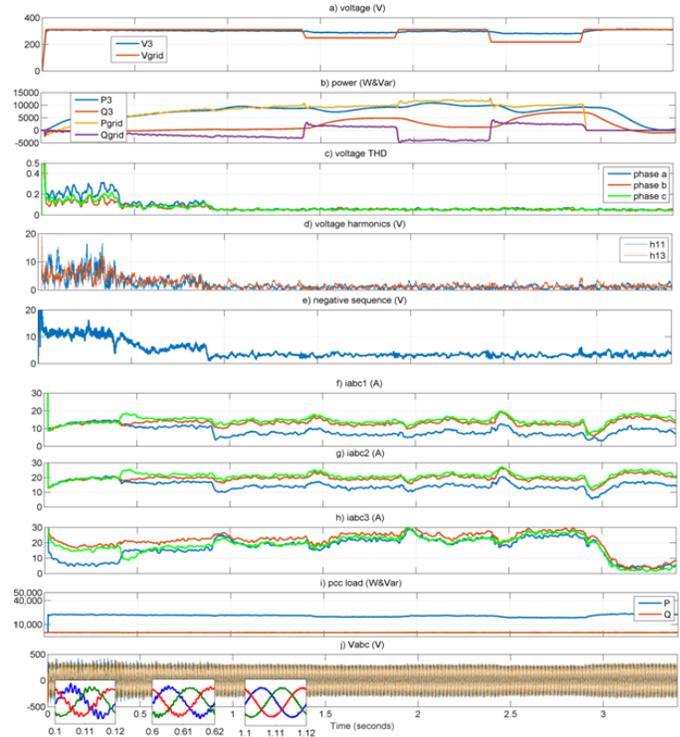


Fig. 11. a) The network voltage and PCC voltage magnitude. b) The power of bus 3 and grid. c) Voltage THD in PCC bus. d) The magnitude of 11th and 13th voltage harmonics. e) Negative sequence voltage of PCC bus. f) The output currents of inverter 1. g) The output currents of inverter 2. h) The output currents of inverter 3. i) The PCC Load power. j) Instantaneous voltages of PCC.

ities on different IBDGs in the MG improves compensation performance and the harmonics distortion and voltage unbalance are divided between DGs appropriately. In the primary level, load compensation factor of each DG is identified considering of its extra capacity. The system has the following applications and capabilities. Tracking of reference currents, compensation voltage harmonics and voltage unbalance at SLB. Simulation result proves the efficiency of the proposed method in different situations.

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