

New switched-capacitor multilevel converter with reduced elements

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This paper presents a new switched-capacitor multilevel converter (SCMC), which is able to produce any levels at output voltage waveform. This topology can increase the value of input dc voltage sources using the switched-capacitor units. In the proposed SCMC topology, as the numbers of switched-capacitor unit increase, the voltage gain and the number of generated levels is increased. The main merit of proposed SCMC topology is an inherent voltage balancing of capacitors. The proposed SCMC structure is compared with traditional multilevel converters. The comparison results verify that the presented SCMC structure needs lower dc voltages sources, switches, and capacitors. The mathematical analysis of standing voltage on switches and different kinds of power losses are provided. In order to verify the performance of the presented SCMC topology, the experimental results for a typical 13-level converter are provided. © 2020 Journal of Energy Management and Technology

keywords: Multilevel converter, Switched-capacitor, Standing Voltage, Power losses, Voltage balancing.

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NOMENCLATURE

V_{sw} Voltage on switches.

$N_{step,sym}$ Index for hub's input energy carrier.

$N_{step,asym}$ The number of produced steps using the asymmetric method.

y The numbers used switched-capacitor units in each side of SCMC.

$P_{c,IGBT}$ Conduction losses of IGBT.

$P_{c,anti}$ Conduction losses of antiparallel diode.

$V_{on,IGBT}$ On-state voltage drop of IGBT.

$V_{on,anti}$ On-state voltage drop of the antiparallel diode.

R_{IGBT} Resistance of IGBT and an antiparallel diode.

R_{anti} Resistance of antiparallel diode.

$N_{on,IGBT}$ The number of on-state IGBTs in the current path.

$N_{on,anti}$ The number of on-state antiparallel diodes in current path.

E_{on} The energy losses during the on the state of a typical switch.

E_{off} The energy losses during the off state of a typical switch.

$P_{sw,off}$ The switching losses during turn-off.

$P_{sw,on}$ The switching losses during turn-on.

t_{on} Turning on time of switches.

t_{off} Turning off time of switches.

N_{on} The number of on state switch.

N_{off} The number of off state switch.

P_{ripple} The ripple losses of capacitors.

N_{sw} Number of switches.

N_{cap} Number of capacitors.

N_d Number of diodes.

N_{dc} Number of dc voltage sources.

P_{out} Output power.

P_{in} Input power.

η Efficiency.

1. INTRODUCTION

In the recent decade, multilevel converters topologies and their applications in the industry have been extensively studied by the researchers. In order to overcome the disadvantages of two and three-level converters such as higher THD of output voltage and voltage on switches, the researchers have been worked on multilevel converters [1–3]. Firstly, traditional multilevel converters were proposed which have been called:

- Flying capacitor multilevel converter (FC)
- Neutral point clamped multilevel converter (NPC)
- Cascade H-bridge multilevel converter (CHB)

FC topology includes back to back connected capacitors along with power switches. In this circuit, as the number of levels increases, the number of used switches, capacitors, and the value of the voltage on switches is increased. Also, the balancing voltage on capacitors is the most important disadvantage of FC topology [4, 5]. In order to improve the disadvantages of FC topology, an improved double flying capacitor multilevel converter has been presented in [6]. The doubling of generated levels is the main merit of this structure and the voltage rating on switches is a fraction of the voltage of the main DC link. However, this topology requires a large number of capacitors and the number of switches in the current path is high.

NPC multilevel converter comprises of switches, diodes, and input dc-link capacitors along with an input dc voltage source. Using a large number of elements and complicated switching strategies are the main demerits of NPC topology [7]. The CHB topology is designed with separated dc voltage sources along with power switches. In this structure, the number of on switches in the current path is high, which increases the power losses. In addition, the number of used dc voltage sources is high, which increases the circuit size and cost [8, 9]. It is noticeable that the conventional topologies cannot boost the value of input dc voltage source.

For improving the CHB topology, several topologies have been studied in [10–16]. Switched-ladder based multilevel converters have been illustrated in [10–13], which comprises of ladder form bidirectional switches and dc voltage sources. In these structures, as the number of bidirectional switches increases, the voltage on the switches is increased. Then, these structures have been recommended for low voltage applications. Another multilevel converter topology has been illustrated in [14]. This topology is based on the cascaded connection of several similar basic units along with an H-bridge at the output. This topology requires many numbers of components and its voltage on switches is high. The other two topologies for multilevel converter have been presented in [15, 16], which utilize a large number of switches and dc voltage sources. It should be mentioned that the proposed multilevel converters in [10–16] are unable to increase the amplitude of input dc voltage source.

For renewable energy sources such as photovoltaic systems, several high voltage gain multilevel converters have been recommended in [17–20]. Two switched-capacitor multilevel converters based on the series-parallel connection of switched-capacitors have been illustrated in [17, 18]. The proposed switched-capacitor topology in [17] can be used in bidirectional power flow applications. However, the proposed topology in [18] is usable in unidirectional power flow applications and cannot be used in inductive load. In these structures, as one capacitor is added, two levels are increased in output voltage waveform. Then, these structures require higher capacitors for generating many numbers of levels, which is an important disadvantage. Another generalized topology of the hybrid switched-capacitor multilevel converter has been studied in [19]. This structure needs higher numbers of dc voltage sources. The capability of voltage boosting and the inherent voltage balancing of capacitors is the main merits of proposed topologies in [17–19].

In order to overcome the demerits of proposed multilevel converters in [10–20] and conventional topologies, a new switched-capacitor based multilevel converter is illustrated in this paper. The performance of proposing basic structure is studied in section 2. In section 3, the proposed switched-capacitor multilevel converter is analyzed. The mathematical analysis of voltage on switches and power losses are illustrated in sections 4 and 5,

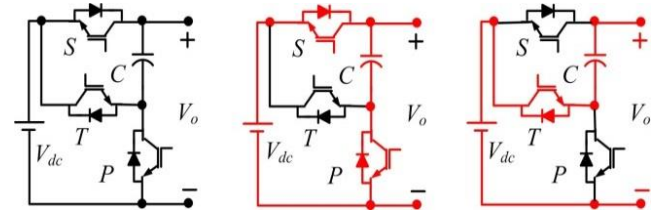


Fig. 1. (a) The topology of switched-capacitor dc-dc converter, (b) current path in the first operation mode, (c) current path in the second operation mode.

respectively. In order to investigate the advantages of proposed topology, comparison results are presented in section 6. Finally, the operation of the proposed SCMC structure is validated using the experimental results of a 13-level converter.

2. PROPOSED BASIC UNIT FOR SWITCHED-CAPACITOR MULTILEVEL CONVERTER

Fig. 1 illustrates the topology of the conventional switched-capacitor DC-DC converter, which includes one input dc voltage source, three unidirectional switches along with a capacitor. This converter has two operation modes. When the switches S and P are turned on, the dc voltage source will be in parallel with the capacitor and the capacitor is charged to V_{dc} . In this state, the output voltage is equal to V_{dc} . In the second mode, the switch T is turned on and the capacitor will be discharged. In this mode, the value of the output voltage will be $2V_{dc}$. Then, the topology of the conventional switched-capacitor DC-DC converter can produce two positive levels ($+V_{dc}$, $+2V_{dc}$) and increase the value of input voltage.

Fig. 2 indicates the basic unit of presented multilevel converter. This structure comprises two switched-capacitor dc-dc units along with six switches ($K_1, K_2, K_3, K_4, K_5, K_6$). The used dc voltage sources have been named $V_{dc,1}$ and $V_{dc,2}$. Moreover, the used capacitors have been named C_1 and \hat{C}_1 . Table 1 illustrates the switching states and charging or discharging of capacitors for generating all possible steps. In order to clarify the switching states of the proposed basic unit for generating the levels, the current path of four levels is indicated in Fig. 3. Fig. 3(a) illustrates the current path for generating step zero. In this step, the switches $K_2, K_5, K_3, S_1, P_1, M_1$, and N_1 are turned on and the capacitors C_1 and \hat{C}_1 are charged. The current path for producing step $+2V_{dc,1}$ is shown in Fig. 3(b). Based on this figure, the switches $K_2, K_6, K_4, T_1, M_1, N_1$ are in ON state and the capacitor \hat{C}_1 are charged. In Fig. 3(c), when the switches $K_1, K_6, K_3, S_1, P_1, M_1, N_1$ are turned on, the capacitors C_1 and \hat{C}_1 are charged and the output voltage will be $+V_{dc,2}$. According to Fig. 3(d), it is clear that the switches K_2, K_6, K_3, T_1, X_1 should be turned on for producing the step $+(2V_{dc,2} + 2V_{dc,1})$. In the presented basic unit, the voltage on the switches is obtained using the following equations:

$$V_{K1} = V_{K2} = 2V_{dc,1} \quad (1)$$

$$V_{K3} = V_{K4} = 2V_{dc,2} \quad (2)$$

$$V_{K5} = V_{K6} = 2(V_{dc,1} + V_{dc,2}) \quad (3)$$

$$V_{S1} = V_{T1} = V_{P1} = V_{dc,1} \quad (4)$$

$$V_{M1} = V_{X1} = V_{N1} = V_{dc,2} \quad (5)$$

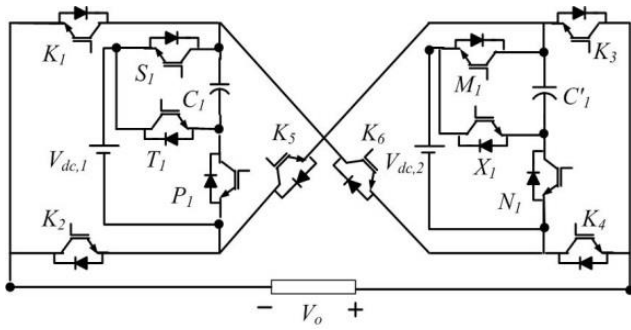


Fig. 2. The topology of proposed basic structure of high voltage gain multilevel converter.

The total value of the voltage on switches of proposed basic unit topology is equal to:

$$V_{sw} = 11(V_{dc,1} + V_{dc,2}) \quad (6)$$

Table 1. ON-state switches and charging capacitors of the proposed basic structure of high voltage gain multilevel converter

| No. | ON Switches | Charging Capacitors | V_o |
|-----|-------------------------------------|-----------------------|----------------------------|
| 1 | $K_2, K_5, K_3, S_1, P_1, M_1, N_1$ | C_1 and \dot{C}_1 | 0 |
| 2 | $K_2, K_6, K_4, S_1, P_1, M_1, N_1$ | C_1 and \dot{C}_1 | $+V_{dc,1}$ |
| 3 | $K_2, K_6, K_4, T_1, M_1, N_1$ | C_1 | $+2V_{dc,1}$ |
| 4 | $K_1, K_6, K_3, S_1, P_1, M_1, N_1$ | C_1 and \dot{C}_1 | $+V_{dc,2}$ |
| 5 | $K_1, K_6, K_3, S_1, P_1, X_1$ | \dot{C}_1 | $+2V_{dc,2}$ |
| 6 | $K_2, K_6, K_3, S_1, P_1, M_1, N_1$ | C_1 and \dot{C}_1 | $+(V_{dc,2} + V_{dc,1})$ |
| 7 | $K_2, K_6, K_3, T_1, M_1, N_1$ | C_1 | $+(V_{dc,2} + 2V_{dc,1})$ |
| 8 | $K_2, K_6, K_3, S_1, P_1, X_1$ | \dot{C}_1 | $+(2V_{dc,2} + V_{dc,1})$ |
| 9 | K_2, K_6, K_3, T_1, X_1 | — | $+(2V_{dc,2} + 2V_{dc,1})$ |
| 10 | $K_1, K_5, K_3, S_1, P_1, M_1, N_1$ | C_1 and \dot{C}_1 | $-V_{dc,1}$ |
| 11 | $K_1, K_5, K_3, S_1, P_1, T_1$ | C_1 | $-2V_{dc,1}$ |
| 12 | $K_2, K_5, K_4, S_1, P_1, N_1, M_1$ | C_1 and \dot{C}_1 | $-V_{dc,2}$ |
| 13 | $K_2, K_5, K_4, S_1, P_1, X_1$ | \dot{C}_1 | $-2V_{dc,2}$ |
| 14 | $K_1, K_5, K_4, S_1, P_1, M_1, N_1$ | C_1 and \dot{C}_1 | $-(V_{dc,2} + V_{dc,1})$ |
| 15 | $K_1, K_5, K_4, T_1, M_1, N_1$ | \dot{C}_1 | $-(2V_{dc,1} + V_{dc,2})$ |
| 16 | $K_1, K_5, K_4, S_1, P_1, X_1$ | C_1 | $-(V_{dc,1} + 2V_{dc,2})$ |
| 17 | K_1, K_5, K_4, X_1, T_1 | — | $-(2V_{dc,2} + 2V_{dc,1})$ |

3. PROPOSED SWITCHED-CAPACITOR MULTILEVEL CONVERTER

The presented basic unit topology can be extended as illustrated in Fig. 4. As shown in this figure, there is y number of switched-capacitor units on each side. It is important to note that the number of used switched-capacitor units on both sides should be similar. It causes the number of generated levels to be high. The switching and capacitor states for generating all possible levels in the presented SCMC are provided in Table 2. In this topology, the number of produced steps at output voltage waveform is related to the values of two dc voltage sources. The values of dc voltage sources can be adjusted as symmetric and asymmetric. In the asymmetric configuration, the value of dc sources will be selected with equal amplitudes as follows:

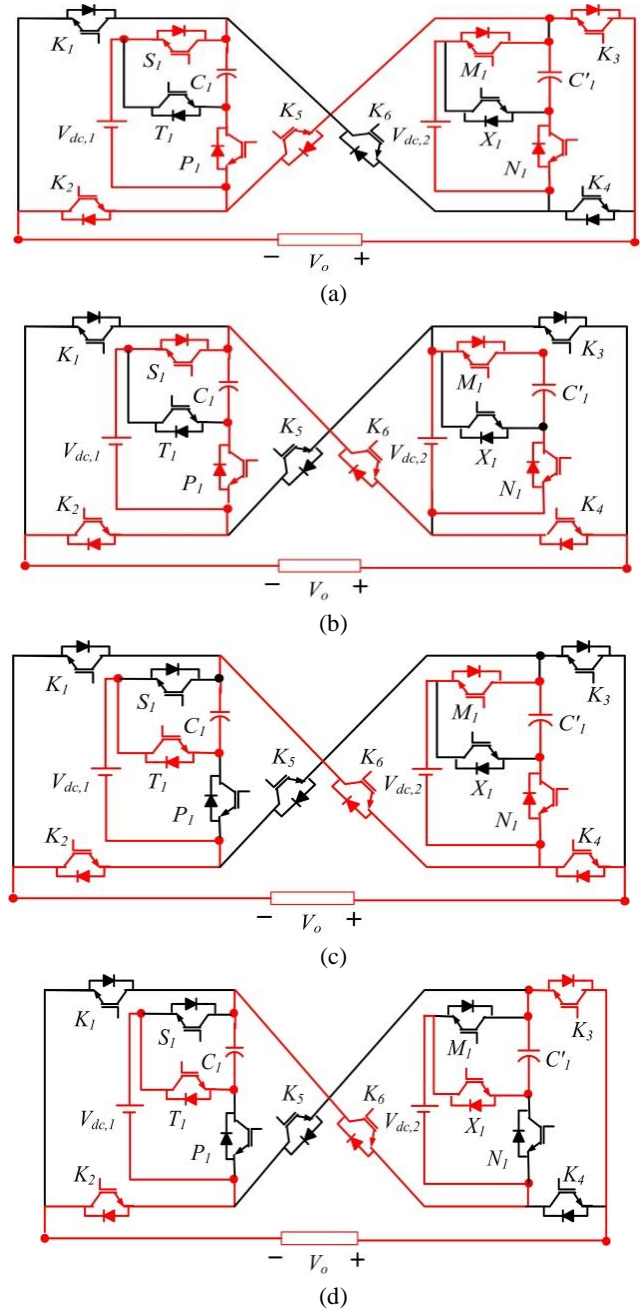


Fig. 3. The current path of proposed basic unit for generating the steps, (a) $V_o = 0$, (b) $V_o = +V_{dc,1}$, (c) $V_o = +2V_{dc,1}$, (d) $V_o = +(2V_{dc,2} + 2V_{dc,1})$.

$$V_{dc,1} = V_{dc,2} = V_{dc} \quad (7)$$

Therefore, the number of steps using the symmetric method ($N_{step,sym}$) will be:

$$N_{step,sym} = 4y + 1 \quad (8)$$

By neglecting the voltage drop on switches, the voltage on all capacitors will be equal to V_{dc} . In other words:

$$V_{Ci} = V_{C'i} = V_{dc} \quad i = 1, \dots, y \quad (9)$$

In addition, the values of dc voltage sources using the asym-

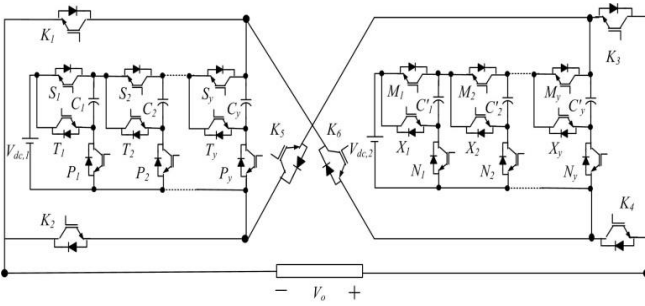


Fig. 4. Presented SCMC topology.

metric method will be selected as follows:

$$V_{dc,1} = V_{dc} \quad (10)$$

$$V_{dc,2} = (y + 2)V_{dc} \quad (11)$$

Therefore, the number of produced steps using the symmetric method ($N_{step,sym}$) will be:

$$N_{step,asym} = 4y + 1 \quad (12)$$

Where y is the number of used capacitors in each side. Using this method, the voltage of capacitors will be:

$$V_{Ci} = V_{dc} \quad i = 1, \dots, y \quad (13)$$

$$V_{C_{y+1}} = (y + 2)V_{dc} \quad i = 1, \dots, y \quad (14)$$

It is clear that the number of produced steps by asymmetric method is higher than symmetric method.

4. CALCULATION OF STANDING VOLTAGE ON THE SWITCHES OF PROPOSED SCMC

Standing voltage on switches is another important parameter in designing multilevel converter. This parameter effects on the circuit cost. In general, the standing voltage on the switches K_1, K_2, K_3, K_4, K_5 and K_6 are obtained as follows:

$$V_{K1} = V_{K2} = 2V_{dc,1} \quad (15)$$

$$V_{K3} = V_{K4} = 2V_{dc,2} \quad (16)$$

$$V_{K5} = V_{K6} = y(V_{dc,1} + V_{dc,2}) \quad (17)$$

Also, the value of standing voltage on other switches of presented SCMC topology will be:

$$V_{Si} = V_{Ti} = V_{dc,1} \quad i = 1, 2, \dots, y \quad (18)$$

$$V_{Pi} = yV_{dc,1} \quad i = 1, 2, \dots, y \quad (19)$$

$$V_{Mi} = V_{Xi} = V_{dc,2} \quad i = 1, 2, \dots, y \quad (20)$$

$$V_{Ni} = yV_{dc,2} \quad i = 1, 2, \dots, y \quad (21)$$

As shown in Eqs. (15)-(21) It is clear that the switches K_5 and K_6 withstand a voltage equal to the maximum value of output voltage. However, other switches tolerate a fraction of the maximum value of output voltage. The total value of standing voltage on switches of proposed SCMC is:

$$V_{sw} = \left(2 + \frac{y}{4} + \frac{y}{(y+1)}\right)(N_{level} - 1)V_{dc} \quad (22)$$

5. CALCULATION OF POWER LOSSES OF PROPOSED SCMC

There are three kinds of power losses which created in the presented SCMC topology as follows:

- Conduction losses
- Switching losses
- Ripple losses of capacitors

Each one above mentioned losses is described as follows:

A. Conduction losses

The conduction losses of an IGBT ($P_{c,IGBT}$) and an antiparallel diode ($P_{c,anti}$) are calculated as follows [11, 13]:

$$P_{c,IGBT} = V_{on,IGBT}I_{out}(t) + R_{IGBT}I_{out}^{\beta+1}(t) \quad (23)$$

$$P_{c,anti} = V_{on,anti}I_{out}(t) + R_{anti}I_{out}^2(t) \quad (24)$$

$V_{on,IGBT}$ and $V_{on,anti}$ are the on-state voltage drop of an IGBT and an antiparallel diode, respectively. In addition, R_{IGBT} and R_{anti} are the resistance of an IGBT and an antiparallel diode, respectively. Moreover, β is a parameter that mentions in the datasheet of transistor. Therefore, conduction losses of switches in the proposed SCMC topology are calculated as follows:

$$P_c = \frac{1}{\pi} \int_0^{\pi} N_{on,IGBT} [V_{on,IGBT}I_{out}(t) + R_{IGBT}I_{out}^{\beta+1}(t)] + N_{on,anti} [V_{on,anti}I_{out}(t) + R_{anti}I_{out}^2(t)] d(\omega t) \quad (25)$$

$V_{on,IGBT}$, $V_{on,anti}$, R_{IGBT} , and R_{anti} are the parameters which are determined by the datasheet of used transistor. $N_{on,IGBT}$ and $N_{on,anti}$ are the number of on-state IGBTs and antiparallel diodes in the current path.

B. Switching losses

In order to calculate the switching losses, the linear approximation of the voltage and current of the switch during OFF-state is used. The energy losses during the on (E_{on}) and off (E_{off}) states of a typical switch are calculated by Eqs. (26) and (27):

$$E_{on} = \int_0^{t_{on}} V_{sw} \cdot I(t) d(t) = \frac{V_{sw} \cdot I \cdot t_{on}}{6} \quad (26)$$

$$E_{off} = \int_0^{t_{off}} V_{sw} \cdot I(t) d(t) = \frac{V_{sw} \cdot I \cdot t_{off}}{6} \quad (27)$$

Using the above equations, the switching losses during turn-off ($P_{sw,off}$) and turn-on ($P_{sw,on}$) in the presented SCMC topology are calculated as follows:

$$P_{on} = N_{on} \cdot f \cdot E_{on} = \frac{N_{on} \cdot f \cdot V_{sw} \cdot I \cdot t_{on}}{6} \quad (28)$$

$$P_{off} = N_{off} \cdot f \cdot E_{off} = \frac{N_{off} \cdot f \cdot V_{sw} \cdot I \cdot t_{off}}{6} \quad (29)$$

Where t_{on} and t_{off} are turning ON and OFF time of switches. Also, N_{on} and N_{off} are the numbers of ON and OFF state of the switch during a fundamental cycle ($1/T$).

Table 2. ON-state switches and charging capacitors of the proposed basic structure of high voltage gain multilevel converter

| ON Switches | Charging Capacitors | V_o |
|---|--|---------------------------|
| $K_2, K_5, K_3, S_1, \dots, S_y, P_1, \dots, P_y, M_1, \dots, M_y, N_1, \dots, N_y$ | $C_1, \dots, C_y, \hat{C}_1, \dots, \hat{C}_y$ | 0 |
| $K_2, K_6, K_4, S_1, \dots, S_y, P_1, \dots, P_y, M_1, \dots, M_y, N_1, \dots, N_y$ | $C_1, \dots, C_y, \hat{C}_1, \dots, \hat{C}_y$ | $+V_{dc,1}$ |
| $K_2, K_6, K_4, T_1, S_2, \dots, S_y, M_1, \dots, M_y, N_1, \dots, N_y$ | $C_1, \dots, C_y, \hat{C}_1, \dots, \hat{C}_y$ | $+2V_{dc,1}$ |
| \vdots | \vdots | \vdots |
| $K_2, K_6, K_3, T_1, \dots, T_y, X_1, \dots, X_y$ | — | $+x(V_{dc,2} + V_{dc,1})$ |
| $K_1, K_5, K_3, S_1, \dots, S_y, P_1, \dots, P_y, M_1, \dots, M_y, N_1, \dots, N_y$ | $C_1, \dots, C_y, \hat{C}_1, \dots, \hat{C}_y$ | $-V_{dc,1}$ |
| $K_1, K_5, K_3, T_1, S_2, \dots, S_y, M_1, \dots, M_y, N_1, \dots, N_y$ | $C_1, \dots, C_y, \hat{C}_1, \dots, \hat{C}_y$ | $-2V_{dc,2}$ |
| \vdots | \vdots | \vdots |
| $K_1, K_5, K_4, T_1, \dots, T_y, X_1, \dots, X_y$ | — | $-x(V_{dc,2} + V_{dc,1})$ |

C. Ripple losses of capacitors

When the capacitors are connected in parallel with input dc voltage sources, the ripple losses of capacitors (P_{ripple}) is created. In general, the losses ripple of capacitors can be calculated by Eq. (30):

$$P_{ripple} = \frac{1}{2T} \left[\sum_{i=1}^y (C_i \Delta V_{C_i} + C'_i \Delta V_{C'_i}) \right] \quad (30)$$

Where, ΔV_{C_i} and $\Delta V_{C'_i}$ are the ripple voltage of capacitors C_i and C'_i , respectively. Then, the total power losses of the proposed SCMC topology (P_{loss}) can be calculated as follows:

$$P_{loss} = P_{c,IGBT} + P_{c,anti} + P_{on} + P_{off} + P_{ripple} \quad (31)$$

Using (31) and (32), the efficiency of the presented SCMC topology will be:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} \quad (32)$$

6. COMPARISON OF PROPOSED SCMC TOPOLOGY WITH OTHER STRUCTURES

In this section, the studied SCMC structure is compared with traditional multilevel converter and those presented in [10–19] and conventional multilevel converters such as FC, NPC, and CHB topologies. The number of required switches (N_{sw}), dc voltage sources (N_{dc}), and capacitors (N_{cap}) in the proposed SCMC topology are:

$$N_{sw} = 6(y + 1) \quad (33)$$

$$N_{dc} = 2 \quad (34)$$

$$N_{cap} = 2y \quad (35)$$

Table 2 compares the features of the proposed 17-level multilevel converter with proposed 17-level converters in [10–20] and conventional structures in terms of the number of required switches, dc voltage sources, diodes, capacitors, and voltage on switches. Based on this table, it is clear that the number of required switches in the proposed 17-level converter and proposed topology in [12] is less than other topologies. Compared to the proposed multilevel converters in [17–20], FC and NPC topologies, the presented 17-level converter needs lower capacitors. The studied 17-level converter does not require power diodes. However, NPC and presented the 17-level converter in

[18] require higher diodes. The CHB structure and illustrated 17-level converters in [10–16] require eight dc voltage sources. However, the proposed 17-level converter requires only two dc voltage sources. The total voltage on the switches in per unit (to V_{dc}) in the proposed 17-level converter is less than proposed 17-level converters in [10–15, 17, 19].

According to the provided comparison in table 3, it is clear that the proposed topologies in [10–16] and conventional topologies are unable to boost the amplitude of input dc voltage source. However, the presented topologies in [17–20] can boost the value of input dc voltage source. Moreover, based on the information provided in Table 3, it is clear that the presented topology in [18] cannot be used in bidirectional flow applications which restricts its applications in inductive loads.

All comparison results prove that the proposed topology requires lower power electronic elements in comparison with other topologies which reduce the manufacturing cost, volume and circuit size. Capabilities of voltage boosting and inherent voltage balancing of capacitors are other merits of proposed converter.

Table 3. Comparison of features of the proposed 17-level converter with proposed 17-level converters in [10–20] and conventional structures

| Top. | N_{sw} | N_{cap} | N_d | N_{dc} | V_{sw} (pu.) | Voltage Boosting | Bidirectional power flow applications |
|----------|----------|-----------|-------|----------|----------------|------------------|---------------------------------------|
| FC | 32 | 8 | 0 | 1 | 32 | No | Yes |
| NPC | 32 | 8 | 240 | 1 | 32 | No | Yes |
| CHB | 32 | 0 | 0 | 8 | 32 | No | Yes |
| [10] | 20 | 0 | 0 | 8 | 76 | No | Yes |
| [11] | 20 | 0 | 0 | 8 | 56 | No | Yes |
| [12] | 18 | 0 | 0 | 8 | 48 | No | Yes |
| [13] | 22 | 0 | 0 | 8 | 90 | No | Yes |
| [14] | 20 | 0 | 0 | 8 | 48 | No | Yes |
| [15] | 25 | 0 | 0 | 8 | 56 | No | Yes |
| [16] | 24 | 0 | 0 | 8 | 36 | No | Yes |
| [17] | 25 | 7 | 0 | 1 | 56 | Yes | Yes |
| [18] | 12 | 7 | 14 | 1 | 40 | Yes | No |
| [19] | 16 | 3 | 0 | 2 | 53 | Yes | Yes |
| [20] | 14 | 4 | 2 | 2 | 40 | Yes | Yes |
| Proposed | 12 | 2 | 0 | 2 | 44 | Yes | Yes |

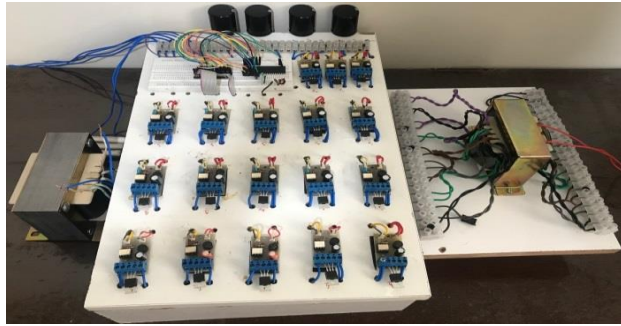
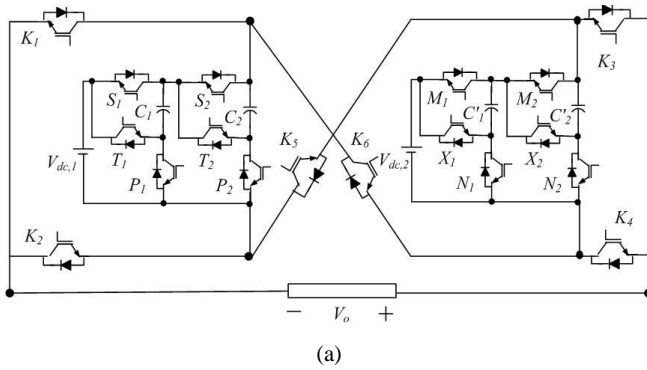


Fig. 5. (a) experimented 13-level converter, (b) photo of the prototype.

7. EXPERIMENTAL RESULTS

In this section, the features of the experimented 13-level converter are studied, which its structure is illustrated in Fig. 5(a). The prototype of the 13-level converter and experimental setup is indicated in Fig. 5(b). The type of used drivers and switches are TLP250 and IRF470, respectively. The value of used capacitors is similar to the values of 3000 μ F.

In order to control the switching pulses, a microcontroller is utilized. It is noticeable that there are several modulation strategies for multilevel converter topologies such as

- Space vector pulse width modulation [21–23]
- Multi-carrier pulse width modulation [24, 25]
- selective harmonic elimination pulse width modulation [26, 27]
- Fundamental frequency modulation [28, 29].

The space vector and multi-carrier pulse width modulation techniques are working in high switching frequencies, which result in extra power losses. However, the selective harmonic elimination and the fundamental frequency modulation are better than the mentioned strategies due to the low switching frequency, which causes the power losses to be reduced. The sinusoidal waveform of output voltage in the multilevel converter using fundamental frequency modulation and its generated levels are illustrated in Fig. 6. It is considered that the elimination of special harmonics is not the aim of this paper. As indicated in this figure, V_{ref} and $\alpha_{1,2,\dots}$ represent the maximum magnitude of reference waveform and switching angles, respectively.

Using fundamental frequency modulation, the switching an-

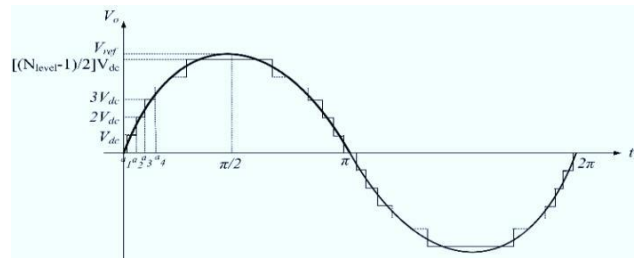


Fig. 6. The waveform of the output voltage of the proposed structure using fundamental frequency modulation.

gles are obtained by the following equation:

$$\alpha_j = \sin^{-1} \left(\frac{2j-1}{2N_{level}} \right) \quad j = 1, 2, \dots, \left(\frac{N_{level}-1}{2} \right) \quad (36)$$

In general, total harmonic distortion (THD) is an operation parameter that provides the harmonics contents of output voltage and current waveforms. The THD for sinusoidal waveform is calculated as follows:

$$THD = \sqrt{\left(\frac{V_{o,rms}}{V_{o,1}} \right)^2 - 1} \quad (37)$$

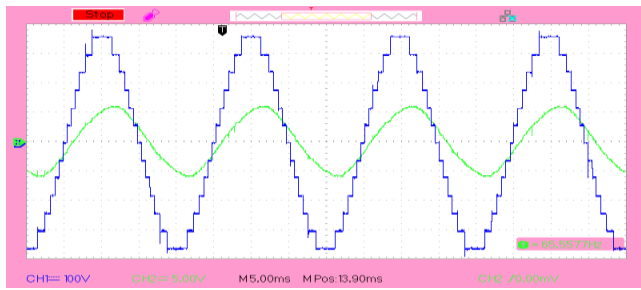
Where, $V_{o,rms}$ and $V_{o,1}$ are the rms and fundamental values of output voltage, respectively. $V_{o,rms}$ and $V_{o,1}$ can be calculated as follows:

$$V_{o,rms} = \frac{V\sqrt{8}}{\pi} \sqrt{\sum_{n=1,3,5,\dots}^{\infty} \left(\sum_{j=1}^{N_{level}} \frac{\cos(n\alpha_j)}{n} \right)^2} \quad (38)$$

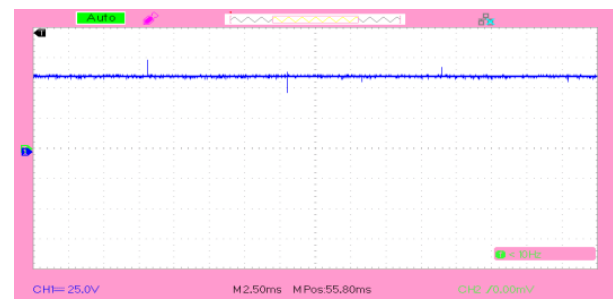
$$V_{o,1} = \frac{V\sqrt{8}}{\pi} \sum_{j=1}^{N_{level}} \cos(\alpha_j) \quad (39)$$

The amplitude of used dc voltage sources has been selected as symmetric with the equal values of 55V. The type of used load is resistance-inductive with the values of R=55 Ω and L=60 mH. The waveforms of output voltage and current along with their harmonic spectrum are indicated in Fig. 7. Based on Fig 7(a) and (c), it is clear that the height of each step is 55 V and the THD of the output voltage is 5.87%. The sum value of input dc voltage sources is 110 V. However, the maximum value of output voltage is almost 330V. It means that the maximum value of output voltage is three times of the sum value of input sources. Therefore, the experimented 13-level converter can act as a boost converter. According to Fig. 7 (a) and (d), the maximum value of output current is 6 A and the THD of output current is 1.07%. The experimental and simulation waveforms of the voltage of the capacitors C1 and C2 are shown in Fig. 8(a) and (b), respectively. These figures prove that the voltage of capacitors is similar with the amplitude of 55 V with voltage balancing capability.

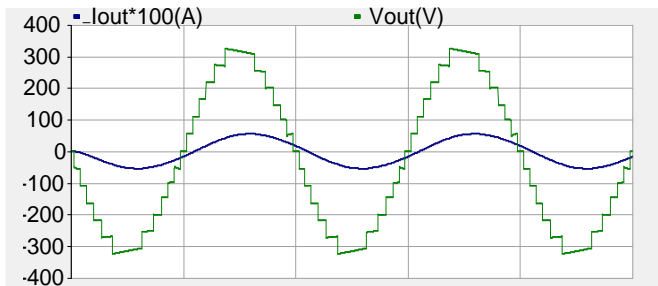
The voltage waveforms of switches of the experimented 17-level converter are indicated in Fig. 9. Fig. 9(a) indicates the voltage waveform of the switch P_2 . According to this figure, it is obvious that the value of the voltage on the switch P_2 is 110V. The voltage waveform on the switch K_2 is indicated in Fig. 9(b). This figure verifies that the maximum voltage on this switch is 165 V. Moreover, the voltage on the switch S_1 is indicated in Fig. 9(c). This figure shows that the maximum voltage on this switch



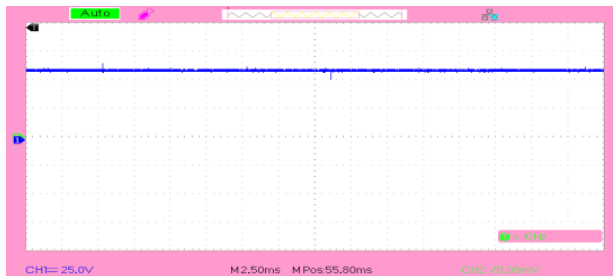
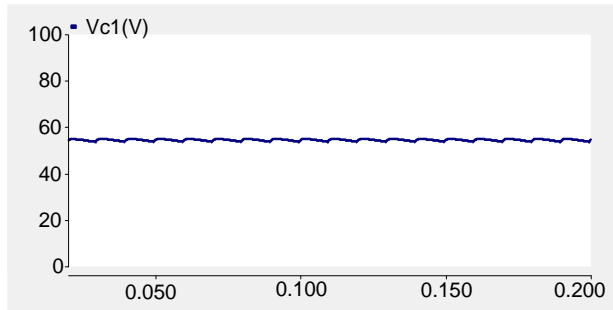
(a)



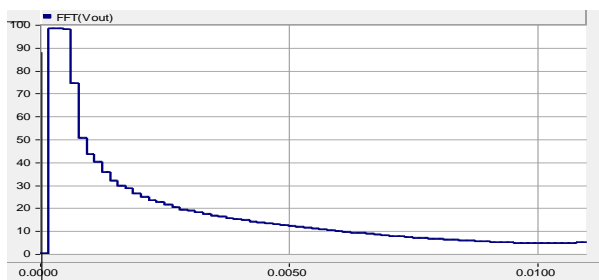
(a)



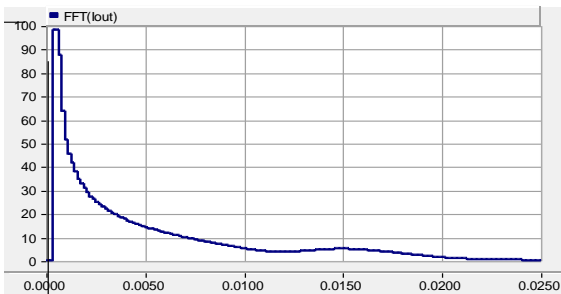
(b)



(b)



(c)



(d)

Fig. 7. (a) The experimental waveforms of output current and voltage, (b) The simulation waveforms of output current and voltage, (c) harmonic spectrum of output voltage, (d) harmonic spectrum of output current.

is 55 V. In addition, Fig. 9(d) illustrates the voltage waveform of the switch K_5 . According to this figure, it is clear that the value of the voltage on the switch K_5 is 330 V. the total maximum voltage on the switches of the experimented 13-level converter is 2090 V.

The values of input and output powers are 1682W and 1608W, respectively. Then, the total value of power losses is almost

Fig. 8. The experimental and simulation waveforms of the voltage of the capacitors (a) C1 and (b) C2.

74W. Therefore, the efficiency of the experimented converter based on the measurements is 95.6%. All simulation results and experimental results verify the performance and mathematical analysis of the studied topology.

8. CONCLUSION

In this paper, a new switched-capacitor multilevel converter was proposed. The proposed structure can operate as a high voltage gain converter using several switched-capacitor units. In this structure, as the number of used switched-capacitors increases, the number of generated output voltage levels and the

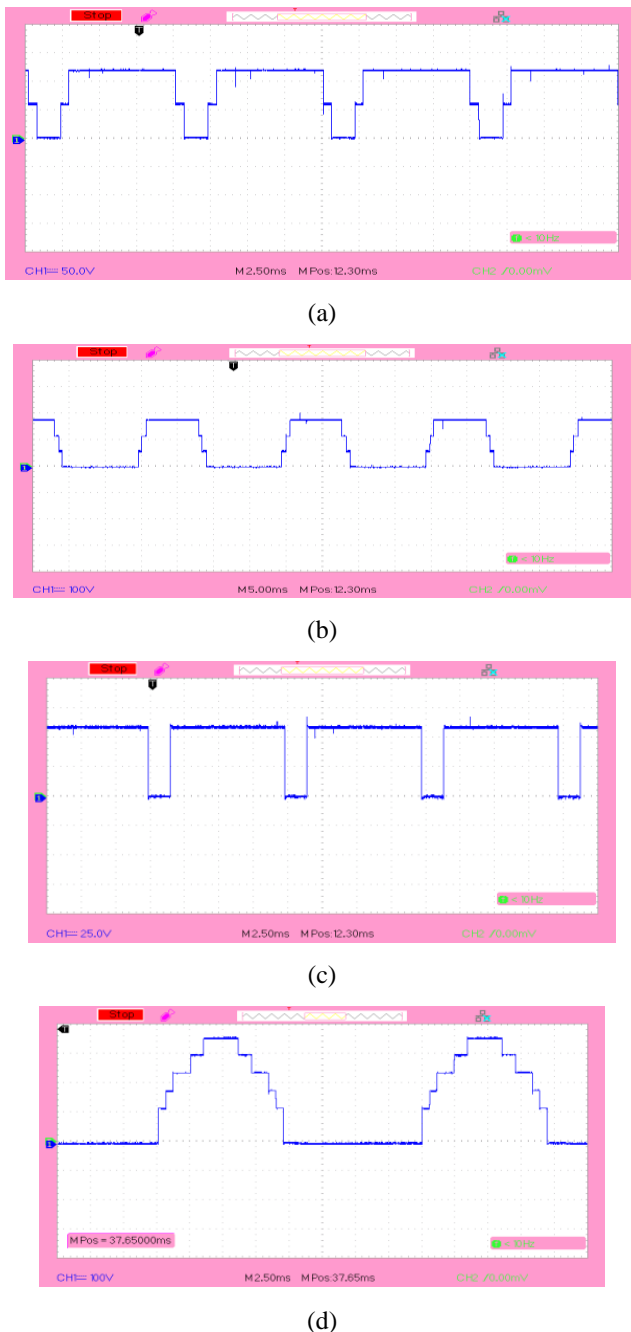


Fig. 9. The voltage of some switches of the experimented 17-level converter (a) P_2 (b) K_2 , (c) S_1 (d) K_5 .

voltage gain of the converter is increased. It was shown that the proposed SCMC converter uses only two high voltage switches. However, the proposed topologies in [15, 17, 18] utilize four high voltage switches in their structures. The proposed topology can be used in inductive loads. However, the proposed SCMC topology in [18] can be used in high power factor loads. It was shown that the proposed SCMC topology needs lower dc voltage sources, capacitors, and switches, which reduces the cost and size. The experimental results for the studied 13-level converter have verified the performance of the proposed converter.

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