A Transformer-Less High Voltage Gain DC-DC Converter Based on Cuk Converter and Voltage-Lift Technique

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Limitations of traditional power sources and the rising need for renewable energy sources have encouraged researchers and manufacturers to enhance the effectiveness of power converters. Recently, numerous high gain topologies have been extensively designed to solve the main issues of the earlier DC-DC boost converters. In this study, a voltage-lift technique is applied to develop a modified high efficiency, high step-up DC-DC converter derived from a typical Cuk converter. The suggested transformer-less circuit also has the benefits of comprising few components and low-cost implementation compared to similar existing converters. Also, the proposed topology effectively boosts voltage gain by including an additional capacitor and a diode. The operational principle and steady-state analysis of the suggested converter in CCM and DCM are discussed in detail. The capabilities of the recommended topology are then demonstrated by mathematical analysis and comparison with previous similar configurations. Furthermore, the parasitic components are considered in the circuit for precisely computing the voltage gain and efficiency. Finally, experimental test results with nearly 210W output power indicate that the proposed converter can be appropriately employed.

keywords: *Transformer-Less Converter, DC-DC Converter, High Step-Up Converter, Voltage-Lift Circuit, Cuk Converter.*

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1. INTRODUCTION

Power plants have relied on fossil fuels to provide electricity ever since the industrial revolution, and the consequent emissions have had a life-threatening effect on nature. Thus, the entire world investigated for new alternatives to create power and respond to the growing demands [1]. As semiconductor switches had first developed in the 1950s, step-up DC-DC converters achieved remarkable enhancements. Next, power field-effect transistors (FETs), capable of switching more efficiently at higher frequencies than BJTs, have allowed for the widespread use of these converters and the gradual improvement of their efficiency and lowering the price and size of the passive elements [2].

There has been a sharp growth of innovative power electronic circuit topologies over the last several years, with diverse applications ranging from the electricity industry to renewable energy sources (RES) and transport systems [3]. The majority of these applications have low voltages on the input side, while they demand a high level of voltages on the output side. Hence, the optimal strategy is using DC-DC converters that can provide varying output voltage gains [4].

Today's applications require DC-DC converters with excellent power density, which can be accomplished by increasing the switching frequency. Nevertheless, the converter's efficiency decreases, and its elements' lifespan reduces as the switching frequency rises. The use of soft switching strategies and stress reduction for semiconductors can be solutions to this issue. [5]. Based on the specifications of the expected utilization and the circuit configuration, DC-DC converters are typically categorized as isolated or non-isolated. Isolated converters may achieve increased voltage by raising the transformer's turns ratio, but doing so reduces efficiency by making the transformer heavier and bulkier. Hence, non-isolated topologies are preferred where isolation is not a necessity. These converters are widely used because of their convenient combination of low cost, small size, and ease of installation [6]. In addition, there are two types of non-isolated high step-up converters: those that use coupled inductors and those that don't. The simplest non-isolated structure without coupled inductor for high voltage gain is the conventional boost converter, but it has several drawbacks, such as high stresses on semiconductors, and the diode reverse recovery issue, which cause less efficiency. Scientists are now focusing on novel DC-DC converter designs to solve these issues [7]. An

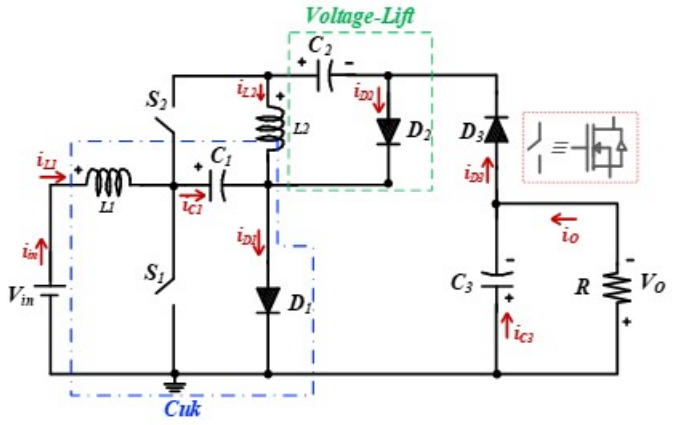

Fig. 1. The suggested converter configuration

even more critical aspect in the design of DC-DC converters is low input current ripple. High input current ripple will affect the lifespan of power resources; decreasing or eliminating this ripple via optimal converter design might extend their usefulness [8].

The importance of DC-DC converters in many fields has led to the development of several configurations, each with its own advantages. A summary of several high-gain converter topologies used for distributed energy sources is provided in [9]. The fundamental purpose of this research is to provide a remarkable comprehensive, comparative, and insightful review of high gain DC-DC converter designs. In this research, converters are separated and sorted into some classes according to their internal specifications. Unlike many review articles focusing on classifying and deriving ways to increase voltage, a particular review article evaluates converters from topological and operational viewpoints. The objective is to identify the most effective methods and converters for specific purposes. In addition, this research suggests a few additional figures of merit that might be used as a benchmark when comparing power electronic converters [10]. Furthermore, an effective Y-source DC-DC converter is suggested in [11]. This converter can provide soft switching features compared to conventional Y-source DC-DC converters. This converter's operational frequency is also increased to lessen the cost of its passive components. As outlined in [12], a high voltage gain converter has been proposed that implements soft-switching and eliminates the need for a transformer. The suggested converter is built on a single-switch dual-inductor boost converter and achieves zero-voltage switching (ZVS) for all its switches, allowing the output diode to turn off naturally. The research conducted in [13] also delves into a thorough investigation of a high step-up DC-DC converter with soft-switching capabilities. All semiconductors achieve Zero Current Switching (ZCS) capability by using the leakage energy of the converter's three-winding coupled inductor, substantially reducing switching losses. Another high-step-up DC-DC converter topology is investigated in [14] that employs a two-winding coupled inductor to boost the output voltage. The proposed design minimizes power losses using a single low ON-state-resistance power switch. Moreover, researchers investigate a recently developed high step-up DC-DC converter with three windings coupled inductors. By using the voltage lift approach and coupled inductors, the suggested converter is capable of producing a significant voltage gain. Despite employing coupled inductors, the input current remains continuous with minimal ripple [15].

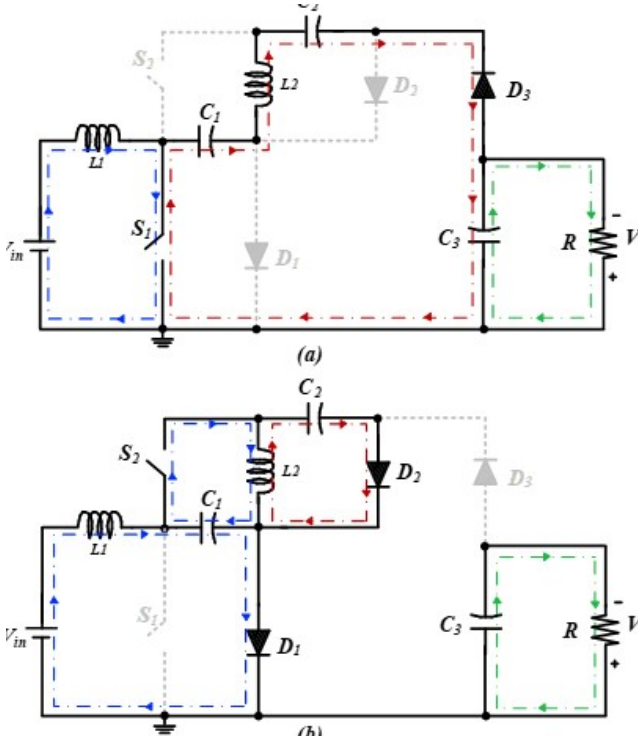

Fig. 2. CCM operating mode current flow directions (a) *Mode I* (b) *Mode II*

An innovative non-isolated step-up converter with the common ground is thoroughly investigated in [16]. The suggested design's voltage and current stress between switches and diodes are less, offering high voltage gain. Moreover, the study of the non-ideal voltage gain of the converter using various components is explored, and comparisons are made to newly proposed converters. Additionally, in renewable energy systems, multiport converters (MPCs) transfer energy from sources like solar panels and wind turbines to storage devices and the larger power grid to regulate the flow of electricity between many different input and output terminals. The topologies of non-isolated MPCs are discussed and reviewed in [17], along with an analysis of their performance based on varying parameters. In another study, a novel coupled inductor and voltage multiplier-based DC-DC converter with high voltage gain is introduced [18]. The suggested converter can boost the output voltage considerably by using the energy stored in the coupled inductor to transmit power. Finally, theoretical analysis and experimental circuit are provided. In addition, the output voltage of a DC-DC converter is maintained at a fixed value regardless of changes in the input voltage using the control methods. Thus, these converters should also use output voltage and input current control mechanisms [19, 20].

Given the widespread usage of DC-DC converters and the consequent need to overcome the drawbacks of the conventional converters, this research proposes an improved transformer-less converter with a straightforward topology and specialized characteristics. The proposed converter is based on the standard Cuk converter, which has a continuous input current with minimal ripple, and employs a voltage-lift circuit to achieve its property of high voltage gain. Moreover, the low component count of the suggested circuit helps keep the system's price down. This converter's output voltage is polarized in the reverse direction from the input ground, making it unique for high performance

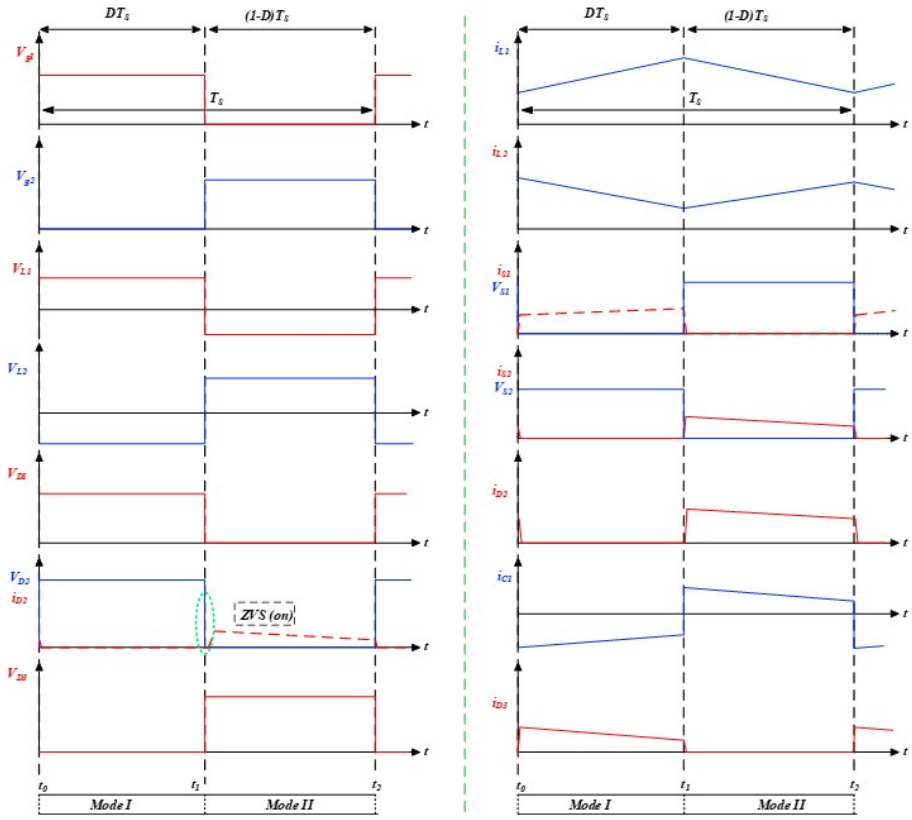

Fig. 3. CCM waveforms for the current and voltage of the proposed converter

applications, including amplifiers, signal generators, and other purposes [21]. Additionally, the input inductor's leakage energy is stored using the passive clamp method, lowering the voltage spike produced by the main switch and increasing the voltage gain. It's worth noting that most of the suggested circuit's semiconductors have low voltage stress, which increases the overall efficiency.

Further statements and investigations of this paper are divided into the following six sections: The steady-state study of the proposed converter's different operational modes, including CCM, BCM, and DCM, are discussed in section 2. The design procedure for the converter's elements is outlined in section 3, and the equations for determining the converter's efficiency and actual voltage gain are provided in section 4. Moreover, in section 5, the suggested converter is compared to the features of recently developed similar converters. Finally, section 6 concludes with a discussion of experimental results from circuit design.

2. TOPOLOGY OF THE SUGGESTED CONVERTER AND OPERATION APPROACHES

Combining the Cuk converter with a voltage-lift circuit (VL), as shown in Fig. 1, attains the suggested converter. It includes two power switches, as well as two inductors, three power diodes, and three capacitors. The operation of the switches is governed by the PWM method that opposes one another. The voltage of the power switch S_1 is also clamped by the snubber circuit formed by capacitor C_1 and diode D_1. More voltage gain is attained gradually, with less stress on components and more straightforward construction, owing to the VL method's exploitation of the properties of energy-storing elements and a suitable switching design. As a result, the recommended converter operates with a high voltage gain in step-up mode. The performance of this converter in its different operation modes (CCM, BCM, and DCM) and equations related to the components' current is discussed in the following subsections. The steady-state computations are performed using the following simplified assumptions to facilitate the analysis.

- All components of the circuit are ideal.
- The capacitors' voltage remains constant during each switching interval since they are sufficiently large.
- The output voltage is expected to be stable since the suggested converter operates in a steady state.
- Current ripples of the inductors are disregarded since they are sufficiently large.

A. CCM Investigation

Two intervals are designated for the proposed converter operation in CCM during the switching times, assuming that both power switches have a duty cycle of 50% and perform in the opposite direction. The directions of the current flowing through the converter at distinct intervals are shown in Fig. 2. Fig. 3 also displays the current and voltage waveforms of the circuit elements driven by the converter's continuous mode of operation. The equations of the suggested converter for each interval (*Mode I*, *Mode II*) are discussed in the following.

Mode I: This mode is activated at time $t = t_0$ when S_1 is on (as seen in Fig. 2(a)). Throughout this time, diode D_3 is active, while S_2, D_1 and D_2 are turned off. The current flowing into inductor L_1 increases since its voltage is positive; hence, it stores

energy. In addition, capacitor C_3 is charged, whereas capacitors C_1 and C_2 are discharged. Furthermore, the inductor L_2 is losing charge. The end of this mode will occur at the instant that the gate signal of S_1 is deactivated ($t = t_1$). Based on the equivalent circuit operating in this mode, the following can be deduced:

$$V_{L1} = V_{in} \quad (1)$$

$$V_{L2} = V_{C1} + V_{C2} - V_O \quad (2)$$

$$V_O = V_{C3} \quad (3)$$

Mode II: As S_1 is turned off, S_2, D_1, and D_2 begin conducting simultaneously when $t_1 < t < t_2$. At this duration, energy is being stored in the inductor L_2. Capacitors C_1 and C_2 are charged, and the energy stored in inductor L_1 is released when the current sloped down, turning the inductor's voltage negative. Moreover, the output capacitor, C_3, is also involved in discharging and delivering the load current. Fig. 2(b) displays the mode of current flow at this time. Once the S_1 starts conducting, this mode is ended ($t = t2$). The suggested converter circuit fulfills the following equations while operating in the second mode:

$$V_{L1} = V_{in} - V_{C1} \quad (4)$$

$$V_{L2} = V_{C1} = V_{C2} \quad (5)$$

$$V_O = V_{C3} \quad (6)$$

Using the converter's equations in both operating modes and the volt-second rule applied to inductor L_1, we get the following:

$$\int_0^{DT_S} V_{L1}dt + \int_{DT_S}^{T_S} V_{L1}dt = 0 \quad (7)$$

$$V_{C1} = \frac{V_{in}}{1-D} \quad (8)$$

Similarly, by using the volt-second rule to the L_2, the following equations are obtained:

$$\int_0^{DT_S} V_{L2}dt + \int_{DT_S}^{T_S} V_{L2}dt = 0 \quad (9)$$

$$V_O = \frac{1+D}{D} V_{C1} \quad (10)$$

By employing the presented equations, the circuit's output voltage and its optimum gain in CCM (M_{CCM}) are determined:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{D+1}{(1-D)D} \quad (11)$$

B. BCM Investigation

The proposed converter is studied in the boundary conduction mode to consider the continuity conditions of the circuit's inductors and input currents. Besides the input current value going to zero at $t = t_1$, BCM analysis is similar to CCM. The waveform of the current passing through the inductor L_1, which is equivalent to the converter's input current, is displayed in Fig. 4. The following equations are obtained if the current ripple value of inductor L_1 is assumed to be Δi_{L1}:

$$\int_0^{I_{L1MAX}} di_{L1} = \int_0^{DT_S} \frac{1}{L_1} V_{L1}dt \quad (12)$$

$$\Delta i_{L1} = \frac{V_{in}DT_S}{L\_1} \quad (13)$$

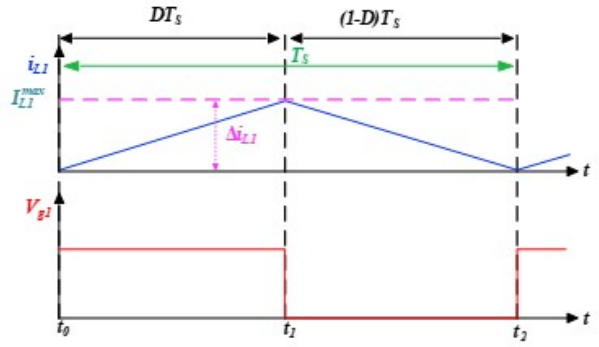

Fig. 4. Current waveform of inductor L_1 in BCM

On the other side, the Eq. (14) can be used to get the average current of the inductor L_1:

$$I_{L1} = \frac{\Delta i_{L1}}{2} \quad (14)$$

This means that:

$$I_{L1} = -\frac{V_{in}DT_S}{2L_1} \quad (15)$$

$$L_1^{BCM} = \frac{V_{in}DT_S}{2I_{L1}} \quad (16)$$

As the average input current is equal to the average current through the L_1, the Eq. (17) is deduced:

$$L_1^{BCM} = \frac{RD^3(1-D)^2}{2f_s(1+D)^2} \quad (17)$$

Therefore, if the value of L_1 lowers below Eq. (17), the converter switches to the DCM. Moreover, the value of L_2 can be obtained in the same way as follows:

$$L_2 = \frac{RD(1-D)^2}{2f_s(1+D)} \quad (18)$$

Fig. 4 also reveals that the average inductor current must be above 50% of the current ripple for CCM operation ($2I_{L1} > \Delta i_{L1}$). Moreover, the time constant τ_L is specified as $\tau_L = Lf_s / R$ to get the normalized inductor [22]. Consequently, inductors L_1 and L_2 have the following boundary states:

$$\begin{cases} \tau_{L1B} = \frac{D^3(1-D)^2}{2(1+D)^2} \\ \tau_{L2B} = \frac{D(1-D)^2}{2(1+D)} \end{cases} \quad (19)$$

Fig. 5 illustrates the relation between τ_L vs. D based on Eq. (19). Hence, CCM operation occurs when $\tau_L > \tau_{LB}$, while DCM operation occurs otherwise.

2.3. DCM Investigation

This mode gives the converter access to three different time intervals during which it may operate in a period; the first two are the same as those featured in the CCM. During the third time interval, the input or current via the inductor L_1 becomes zero. This indicates that all semiconductors have been disabled. Fig. 6 depicts the DCM waveform of the converter's input current. The following is determined using the volt-second law for the inductor L_1 when the converter's input current is assumed to be zero at $D'T_S$:

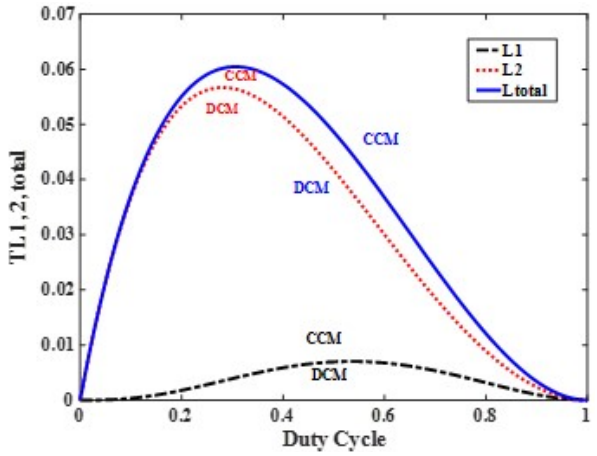

Fig. 5. Suggested converter's boundary states

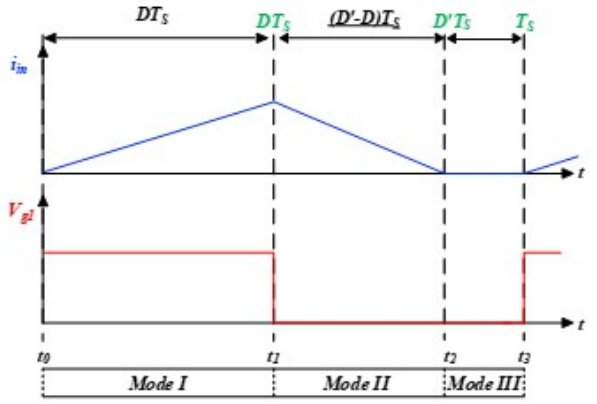

Fig. 6. DCM waveform of the converter's input current

$$\begin{cases} \int_0^{DT_S} V_{L1}dt + \int_{DT_S}^{D'T_S} V_{L1}dt = 0 \\ V_{C1} = \frac{V_{in}D'}{D'-D} \end{cases} \quad (20)$$

The similar presumption can also be made with the inductor L_2:

$$\begin{cases} \int_0^{DT_S} V_{L2}dt + \int_{DT_S}^{D'T_S} V_{L2}dt = 0 \\ V_{C1}(D'+D) = V_O D \end{cases} \quad (21)$$

In conclusion, the above equations yield the following relation for the converter gain in DCM:

$$M_{DCM} = \frac{D'(D'+D)}{D(D'-D)} \quad (22)$$

As demonstrated in Eq. (22), the voltage gain equation in CCM is achieved by setting $D' = 1$. As a result, D' must be less than 1 in DCM.

3. CONVERTER'S COMPONENTS DESIGN

Knowing the capacitor and inductance values, as well as the voltage stress and maximum current of the semiconductors, and selecting the suitable model of these components, is essential for designing and implementing a converter's circuit. The analysis of the aforementioned factors is thus studied in this section. Following the operating principle of the recommended converter, voltage stresses on the switches are stated as follows:

$$V_{S1} = \frac{V_{in}}{1-D} \quad (23)$$

$$V_{S2} = \frac{V_O}{1+D} \quad (24)$$

In addition, the currents of power switches can be computed using the following equations:

$$I_{S1} = \frac{2I_O}{D(1-D)} \quad (25)$$

$$I_{S2} = \frac{I_O}{D(1-D)} \quad (26)$$

The proposed converter has also the following equations for the voltage stress on the diodes and their current:

$$V_{D1} = V_{C1} = \frac{V_{in}}{1-D} \quad (27)$$

$$V_{D2} = V_{C2} - V_{L2} = \frac{V_O}{1+D} \quad (28)$$

$$V_{D3} = V_O \quad (29)$$

$$i_{D1} = i_{L1}^{II} \quad (30)$$

$$i_{D2} = i_{C2}^{II} \quad (31)$$

$$i_{D3} = i_{L2}^{I} \quad (32)$$

A. Inductors and Capacitors Design

To determine the inductance of a converter, it is necessary to know the required current ripple and the operating circumstances of the circuit (DCM or CCM). Moreover, optimal effectiveness and performance from the inductors were prioritized by considering the minimal values of $\Delta i_L = 0.3 I_L$ for current ripples in the proposed converter throughout the design phase. Hence, the Eq. (17) and Eq. (18) can be utilized to obtain the values of L_1 and L_2. The maximum and average currents of the inductors are also as follows:

$$\begin{cases} I_{L1} = I_{in} \\ I_{L1}^{\max} = I_{L1} + \frac{\Delta i_{L1}}{2} \end{cases} \quad (33)$$

$$\begin{cases} I_{L2} = \frac{I_O}{D} \\ I_{L2}^{\max} = I_{L2} + \frac{\Delta i_{L2}}{2} \end{cases} \quad (34)$$

Capacitors are considered components that hold constant voltage since it is evident that sensitivity on the capacitor voltages would affect the system performance. The capacitors C_1 and C_3 voltage relations have been derived in Eq. (8) and Eq. (11) as a result of the previous investigations. In addition, the voltage stored in capacitor C_2 is the same as that stored in capacitor C_1:

$$V_{C2} = \frac{V_{in}}{1-D} \quad (35)$$

The following is taken into account while identifying the capacitors' voltage ripple:

$$\Delta V_C < 0.01 V_C \quad (36)$$

As a result, it is feasible to compute the values of the capacitors by considering both the acceptable voltage ripple and the current passing through them:

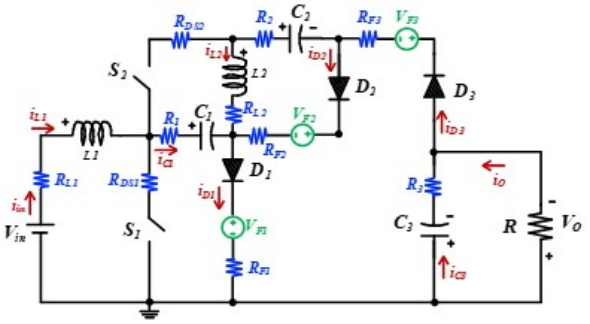

Fig. 7. Parasitic components in the circuit of the presented converter

$$\begin{cases} I_{C1}^{II} = \frac{I_O}{1-D} \\ C_1 = \frac{I_{C1}DT}{\Delta V_{C1}} \end{cases} \quad (37)$$

$$\begin{cases} I_{C2}^{II} = \frac{I_O}{1-D} \\ C_2 = \frac{I_{C2}DT}{\Delta V_{C2}} \end{cases} \quad (38)$$

$$\begin{cases} I_{C3}^{II} = I_O \\ C_3 = \frac{I_{C3}(1-D)T}{\Delta V_{C3}} \end{cases} \quad (39)$$

4. PARASITIC ELEMENTS IMPACT

On the presumption that the proposed converter circuit is ideal, the previous sections derived the equations of the system design and steady-state analysis of the converter. This section modifies the circuit to include resistance and parasitic elements to test the converter's efficiency, total losses, and output voltage during actual operating circumstances, as shown in Fig. 7. As a result, the following descriptions are used to define these resistances:

R_{DS1} and R_{DS2} represent the power switches resistance while switches S_1 and S_2 are activated.

L_1 and L_2 inductor ESRs are denoted by R_{L1} and R_{L2}, respectively.

The threshold voltages of the diodes and their related forward resistances are shown by V_{F1}-V_{F3} and R_{F1}-R_{F3}, respectively.

The capacitors' ESR values are indicated by R_1 through R_3.

A. Study of Real Voltage Gain

Whenever the internal resistances of the components are factored into the circuit, the computation process of the actual voltage gain of the suggested converter is identical to the ideal voltage gain derived in subsection 2.1. What's different this time is that resistances are entered into the formulas. Hence, the following equations can be stated utilizing the conduction paths of the suggested circuit in *Mode I* of the CCM:

$$V_{L1} = V_{in} - R_{L1}i_{in} - R_{DS1}i_{S1} \quad (40)$$

$$V_{L2} = V_{C1} + V_{C2} - V_O - R_{L2}i_{L2} - R_1 i_{L2} - R_2 i_{L2} - R_{F3}i_{L2} - R_{DS1}i_{S1} - V_{F3} \quad (41)$$

$$V_O = V_{C3} + R_3 i_{C3} \quad (42)$$

In *Mode II*, the converter's equivalent circuit can correspondingly be modelled using KVLs, allowing us to reach the following:

$$V_{L1} = V_{in} - V_{C1} - R_{L1}i_{in} - R_1 i_{C1} - R_{F1}i_{F1} - V_{F1} \quad (43)$$

Table 1. The parasitic element features of the converter

Elements/Parameters	Values
R_{Fi}	0.05Ω
V_{Fi}	1V
$R_{1,2}$	0.2Ω
R_3	0.43Ω
R_{L1}	0.006Ω
R_{L2}	0.1Ω
C_S	310pF

$$V_{L2} = V_{C2} - R_{L2}i_{L2} + R_2 i_{C2} + V_{F2} + R_{F2}i_{C2} \quad (44)$$

It is feasible to figure out the real gain of the converter by using the volt-second law for the inductors in the circuit:

$$V_{C1} = V_{in}\left(\frac{1}{1-D} - \frac{R_{F1}+2}{L_2 f_s}\right) + V_O\left(-\frac{R_{L1}}{R_1}\left(\frac{(1+D)(2-D)}{(1-D)^2}\right) - \frac{R_1(1+D)}{R(1-D)}\right) \quad (45)$$

$$M_{real} = \frac{\left(\frac{1+D}{D(1-D)}\right) + \frac{1}{V_{in}}[V_{F1} + V_{F2} + V_{F3}]}{e} \quad (46)$$

where

$$\begin{cases} e = 1 + \frac{1}{R}[aR_{L1} + bR_1 \\ +c(R_{L2} + R_2 + R_{D1} + R_{F3}) + dR_{D2}] \\ a = \frac{(1+D)^2(2-D)}{(1-D)^2 D}, b = \frac{1+D^2}{D(1-D)} \\ c = \frac{1+D(D-1)}{1+D}, d = \frac{D(1+D)}{(1-D)^2} \end{cases} \quad (47)$$

If the resistance values are taken out of the equation, the ideal voltage gain value described in Eq. (11) exactly matches the actual voltage gain value of the converter, as seen by verifying Eq. (46). To further evaluate the influence of parasitic components, Fig. 8 contrasts the actual voltage gain value of the converter with the ideal value. It is clear that when the converter's duty cycle rises, the real voltage gain value falls dramatically compared to the theoretical voltage gain. Due to this, increasing the duty cycle ($D > 0.8$) would not allow the proposed converter to function optimally.

B. Efficiency Analysis

To evaluate the converter performance, it is important to understand the conduction losses caused by the various circuit elements. Furthermore, the effect of current stress on the components in a circuit is increasingly significant when discussing its efficiency. Hence, one must first compute the currents associated with the circuit components before determining the values of losses. Using this information, the following relations are derived for the RMS currents flowing through the diodes of the proposed converter circuit:

$$I_{D1}^{rms} = \frac{I_O\sqrt{1-D}(1+D)}{D(1-D)} \quad (48)$$

$$I_{D2}^{rms} = \frac{I_O}{\sqrt{1-D}} \quad (49)$$

Table 2. Specific details of the designed converter

Elements/Parameters	Descriptions
S_1, S_2	IRFP260N
D_1-D_3	MUR1560
C_1, C_2	470μF / 100V
C_3	470μF / 400V
L_1	400μH-10A
L_2	700μH-5A
R	100Ω
Gate Driver	TLP250
V_{in}	25V
V_{out}	145V
Frequency	40kHz
Output Power	210W

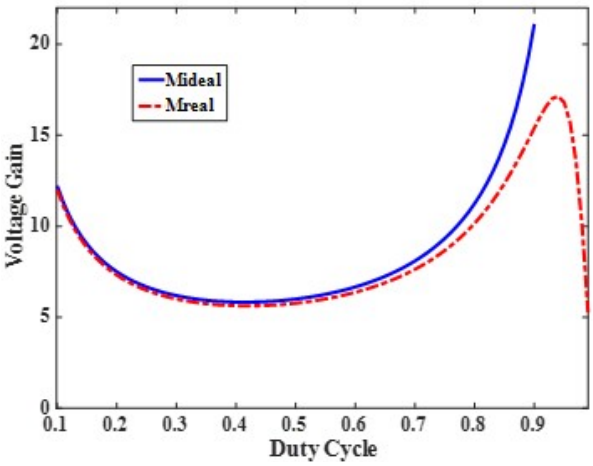

Fig. 8. Proposed converter's real vs. ideal voltage gain

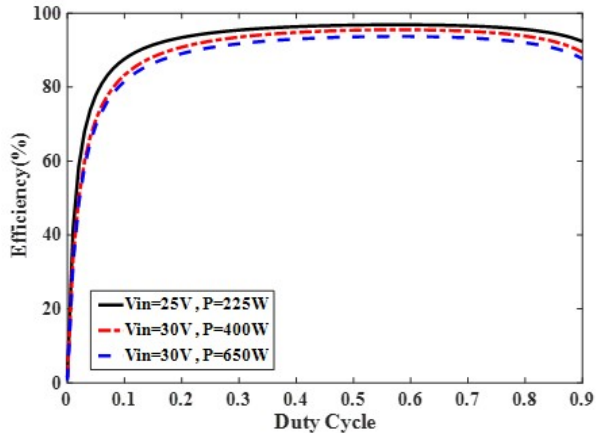

Fig. 9. Duty cycle dependent efficiency curve for the suggested converter

$$I_{D3}^{rms} = \frac{I_O}{\sqrt{D}} \tag{50}$$

Moreover, the average currents of diodes are determined as follows:

$$I_{D1}^{avg} = \frac{I_O(1+D)}{D} \tag{51}$$

$$I_{D2}^{avg} = I_{D3}^{avg} = I_O \tag{52}$$

The following are also relations of the power switches' RMS and average currents:

$$I_{S1}^{rms} = \frac{2I_O}{(1-D)\sqrt{D}} \tag{53}$$

$$I_{S1}^{rms} = \frac{I_O}{D\sqrt{1-D}} \tag{54}$$

$$I_{S1}^{avg} = \frac{2I_O}{1-D} \tag{55}$$

$$I_{S2}^{avg} = \frac{I_O}{D} \tag{56}$$

Determining the efficiency of the suggested converter utilizes the following formula:

$$\eta_{conv} = \left(\frac{P_O}{P_O + P_{loss}}\right) \tag{57}$$

$$P_{loss} = P_{SW} + P_{RF} + P_{VF} + P_L + P_C \tag{58}$$

where power switch losses (P_{SW}), inductor losses (P_L), capacitor losses (P_C), and diode losses (P_{RF} and P_{VF}) all contribute to the overall system losses in the proposed structure. Here's how to determine the P_{SW} [2]:

$$P_{SW} = R_{DS-ON}(I_S^{rms})^2 + \frac{1}{2}f_s(t_{on} + t_{off})I_S^{avg}V_S \tag{59}$$

As a result, the converter switches losses are computed as follows:

$$P_{SW} = \sum_{i=1}^{2} R_{DSi}(I_{Si}^{rms})^2 + \frac{1}{2}f_s(t_{on} + t_{off})I_{Si}^{avg}V_{Si} \tag{60}$$

Because of their short switching times, MOSFETs incur losses whenever they shift from on to off and back again. The symbols t_{on} and t_{off} display the MOSFET on/off transition times. Even though the S_1 has minimal switching losses, the suggested converter fails to have a soft-switching capability for the main switch. It is also conceivable to define the diodes' P_{RF} and P_{VF} in this way:

$$P_{RF} = \sum_{i=1}^{3} R_{Fi}(I_{Di}^{rms})^2 \tag{61}$$

$$P_{VF} = \sum_{i=1}^{3} V_{Fi}I_{Di}^{avg} \tag{62}$$

In addition, the losses of the inductors are calculated as follows:

$$P_L = \sum_{i=1}^{2} R_{Li}(I_{Li}^{rms})^2 \tag{63}$$

In the end, the capacitors' power losses (P_C) are determined in the following manner:

$$P_C = \sum_{i=1}^{3} R_i(I_{Ci}^{rms})^2 \tag{64}$$

Parasitic element values for the suggested converter circuit is listed in Table 1. These numbers are taken from the components used to assemble the circuit. In addition, Fig. 9 shows the suggested converter's duty cycle-based efficiency curve for different power levels. Increasing the converter's power causes the efficiency to decrease, as expected; nonetheless, the suggested converter still has an acceptable efficiency range and is suitable for high-power applications. In addition, if the D is set to 1, a short circuit on the power supply side would prevent any power from reaching the output.

5. COMPARATIVE ANALYSIS

In this part, several comparisons are presented to demonstrate the benefits and characteristics of the proposed converter. The specifications of circuits with similar topologies [22**?** –29] to the one presented are compared in Table 2. This includes the number of elements, the magnitude of voltage gain, and the efficacy of the converters under discussion. The suggested converter contains two power switches in its circuit, although it is more efficient than most other structures. This demonstrates that the semiconductors were not subjected to excessive voltage or current stress.

A comparison between the suggested converter and other converters listed in Table 2 in terms of voltage gain based on the duty cycle is presented in Fig. 10. Although having a lower total number of components, it is visible that the recommended converter has a larger voltage gain than most other topologies that have been investigated. The output voltage gain of the converters described in [22–25] also improves considerably in higher duty cycles. Nevertheless, the drawbacks of the converter performance in greater duty cycles, such as increased losses in the circuit, should also be considered. Fig. 10 also illustrates that the topologies provided in [26, 27] exhibit similar behavior as the proposed circuit, although they have a lower voltage gain and efficiency. The suggested converter has a reasonably large advantage over the converter described in [28], which has a gain equivalent to the conventional boost converter but also has identical flaws. Moreover, the voltage gain of the converter proposed in [29] is substantial; however, it is both costly and inefficient due to its numerous components.

The suggested circuit is investigated further by contrasting the voltage stress on the S_1 with the voltage on the main switches of other elements. Hence, based on each converter's ideal voltage gain (M_{CCM}), Fig. 11 shows the voltage stress ratio on the main switches (V_S/V_{in}). The proposed converter has a lower voltage stress than most of the others under study, and the switch voltage value grows gradually with increasing gain. Therefore, it is obvious that topologies' greater voltage stress on the switches causes an increase in system losses and a fall in efficiency. The converters presented in [22], and [28] have lower switch voltage stress than the suggested structure. Still, the proposed structure's extremely high voltage gain and efficiency have made its application more reasonable and practical.

From the different comparisons discussed in this section, the converter provided in this article has few components, a relatively high voltage gain and efficiency, and voltage stresses on its semiconductors are in an acceptable range. Because of this, the proposed converter may be suggested for use in various high-power industrial applications. By comparing the suggested converter with the traditional boost structure, it becomes clear that the former is a vast improvement in every respect and a viable alternative to the latter.

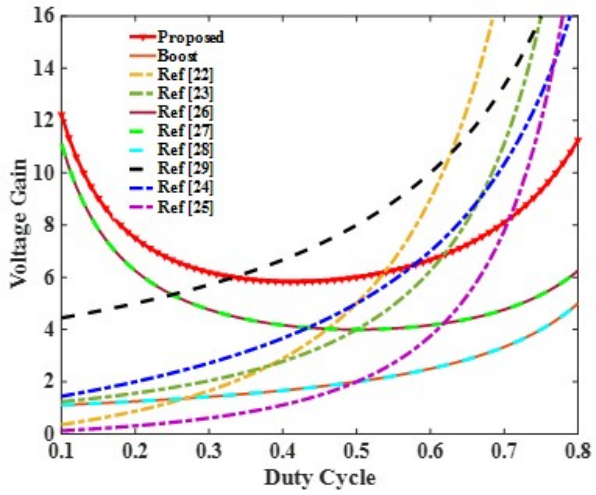

Fig. 10. Gain curve comparing the suggested converter with different structures

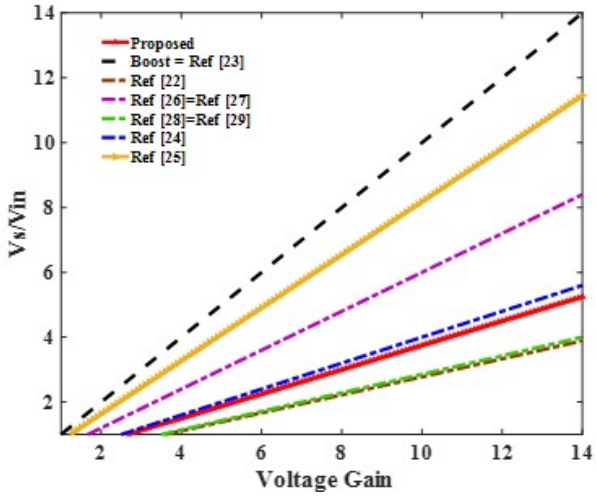

Fig. 11. The voltage stress on switches based on M_{CCM}

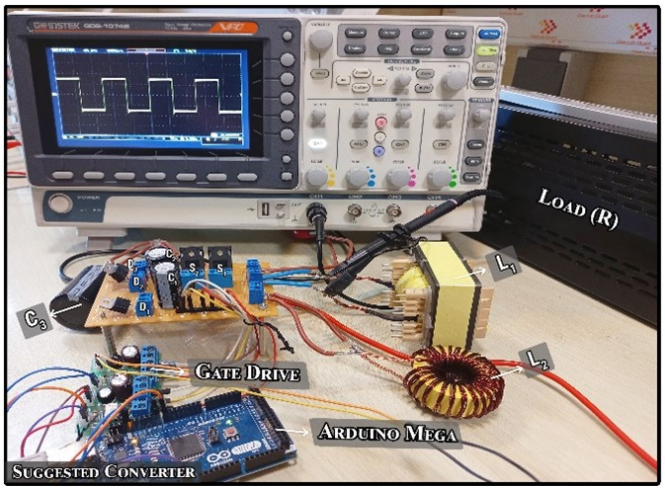

Fig. 12. Experimental setup used to verify the suggested circuit

Table 3. Comparison of presented converter features with other recent studies

Considered researches	M_{CCM}	Voltage stress on switches	Switch Numbers	Diode Numbers	Capacitor Numbers	Inductor Numbers	Efficiency at rated power
Boost Converter	$\frac{1}{1-D}$	MV_{in}	1	1	1	1	89% at 100W
Topology of [23]	$\frac{1}{(1-D)^2}$	MV_{in}	1	5	4	3	93.30% at 150W
Topology of [24]	$\frac{1+3D}{1-D}$	$\frac{MV_{in}}{1+3D}$	2	2	3	3	93.1% at 200W
Topology of [25]	$\frac{D}{(1-D)^2}$	$\frac{MV_{in}(1-D)}{D}$	1	3	3	3	91.4% at 100W
Topology of [22]	$\frac{(3D-D^2)}{(1-D)^2}$	S_1 $\frac{(1-D)M}{(3D-D^2)}V_{in}$	2	3	4	3	92% at 100W
		S_2 $\frac{M}{(3D-D^2)}V_{in}$					
Topology of [26]	$\frac{1}{D(1-D)}$	S_1 $MV_{in}D$	2	3	2	2	89.5% at 50W
		S_2 $\frac{MV_{in}}{(1+D)D}$					
Topology of [27]	$\frac{1}{D(1-D)}$	S_1 $MV_{in}D$	2	2	2	2	92.2% at 40W
		S_2 $\frac{MV_{in}}{(1+D)D}$					
Topology of [28]	$\frac{1}{1-D}$	S_1 $MV_{in}/4$	2	4	5	2	94% at 150W
		S_2 $MV_{in}/4$					
Topology of [29]	$\frac{4}{1-D}$	S_1 $MV_{in}/4$	2	9	6	4	94.1% at 200W
		S_2 $MV_{in}/4$					
Suggested Converter	$\frac{D+1}{D(1-D)}$	S_1 $\frac{MD}{1+D}V_{in}$	2	3	3	2	96.2% at 210W
		S_2 $\frac{MV_{in}}{(1+D)}$					

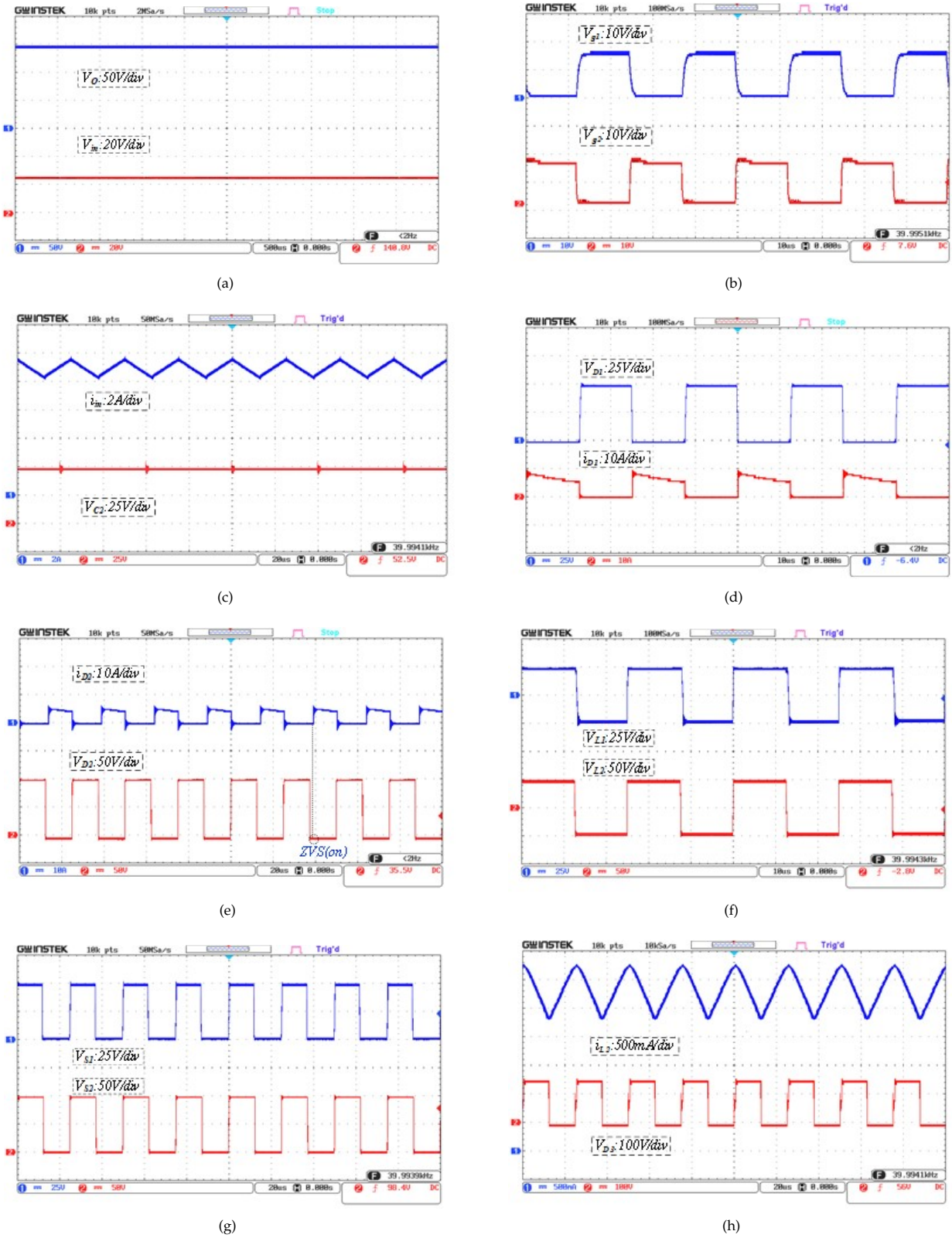

Fig. 13. The suggested structure experimental waveforms

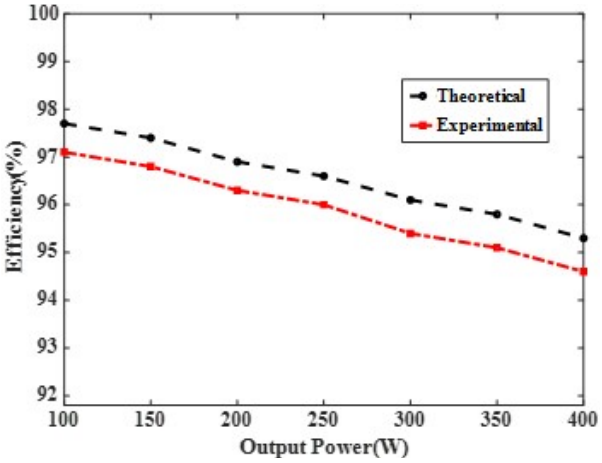

Fig. 14. Efficiency findings of the proposed converter for a range of output powers

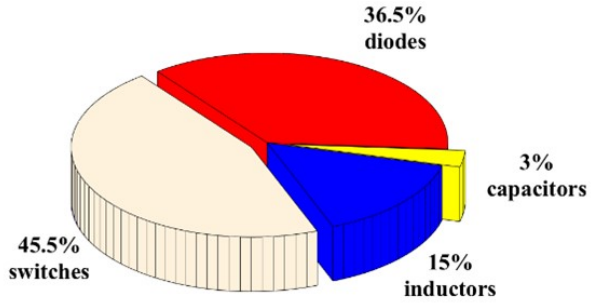

Fig. 15. Distribution analysis of the losses in the suggested converter

6. EXPERIMENTAL FINDINGS

The characteristics of the recommended converter built in the lab are described in this section, and the experimental results have been collected to validate the steady-state assessment. Therefore, as illustrated in Fig. 12, an electrical prototype of the converter with around 210 W output power has been manufactured. The suggested converter's power switches are controlled by an Arduino Mega2560, which provides PWM signals to the gate drivers. Table 3 shows the converter prototype's element specifications and how the topology operated.

Fig. 13 depicts some necessary experimental waveforms obtained by the converter throughout its evaluation. As displayed in Figure 13(a), the output voltage is about 145 volts, which agrees with Eq. (11). In this instance, the ripple of the output voltage is likewise negligible and can therefore be disregarded. The PWM waveforms of the circuit switches (gate voltages) at D = 0.5 with opposing signals are also shown in Fig. 13(b). Fig. 13(c) additionally depicts the input current and capacitor C_2 voltage waveforms. As can be observed, C_2 provides 48.6V, which agrees with Eq. (35), and i_{in} shows an average value of about 8.73A. Hence, the circuit is obviously designed to function in CCM.

The voltage and current of the D_1 are also shown in Fig. 13(d), where its highest voltage value is 49.2V, which corresponds to Eq. (27). Moreover, Fig. 13(e) shows the voltage and current of D_2. 1.5 A is the average value provided by D_2 current, consistent with Eq. (52); and voltage of D_2 is around 97.2V, confirming Eq. (28). In addition, the ZVS state can be determined by analyzing these waveforms. The voltage waveforms of L_1 and L_2 are illustrated in Fig. 13(f). The results confirm the validity of the theoretical analysis performed in CCM and the volt-second rule. Additionally, the voltage waveforms of S_1 and S_2 are displayed in Fig. 13(g). It demonstrates the correction of Eq. (23) and Eq. (24) and shows that the voltage on S_1 is almost 48.5 V, and the voltage on switch S_2 is around 97V. This means the power switches have maximum voltages lower than the V_O. Fig. 13(h) depicts the current and voltage waveforms of L_2 and D_3, both of which are consistent with Eq. (34), Eq. (29).

The theoretical and practical efficiency of the suggested converter is shown in Fig. 14 over a range of output powers. According to this figure, the proposed converter can deliver an output power of about 210W while maintaining an efficiency of around 96.2%. This circuit's excellent efficiency can be attributed to its low number of components and well-thought-out design. While the circuit's efficiency drops dramatically when the converter's power increases, it is still within an acceptable range. Hence, the theoretical study and experimental result indicated that the suggested structure is a wise choice for various applications owing to its high effectiveness and excellent output voltage gain. Furthermore, the recommended converter loss distribution is displayed in Fig. 15. This figure is obtained using the equations calculated in section 4.2. As can be seen, the capacitors have the most minor power loss, but the power switches have the most considerable amount of power loss.

7. CONCLUSIONS

In this research, a modified high-step-up ratio non-isolated DC-DC converter is presented. The standard Cuk converter served as the basis concept for this converter, and the suggested topology uses fewer components and has lower production costs compared to most similar topologies. The described structure employs a VL voltage-boosting circuit to increase the output voltage. Moreover, the recommended converter further enhances circuit efficiency because of the low voltage stress applied to the switches. For proper design, the steady-state evaluations between the components in the CCM and DCM were investigated. The inductance equations for the critical mode (BCM) were also determined. The suggested converter was also compared to those provided in previous papers using different methodologies concerning their output voltage gain, estimated efficiency, and the number of components required to implement the converter. In contrast to previous converters, the proposed converter was shown to have greater voltage gain and appropriate efficiency at CCM. Finally, 210W output power with 40kHz switching frequency laboratory results show the design's usefulness in the actual applications.

8. ACKNOWLEDGMENTS

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REFERENCES

1. Y.-E. Wu and K.-C. Chen, "High Efficiency and High Voltage Conversion Ratio Bidirectional Isolated DC–DC Converter for Energy Storage Systems," Processes, vol. 10, no. 12, p. 2711, 2022.
2. R. Mohajery, H. Shayeghi, F. Sedaghati, A. Bahador, and N. Bizon, "A modified configuration of high step?up non?isolated DC?DC converter with low voltage stress: Analysis, design, and implementation," International Journal of Circuit Theory and Applications, vol. 51, no. 9, pp. 4178–4201, 2023.
3. E. Naderi, S. J. Seyedshenava, H. Shayeghi, "High Gain DC/DC Converter Implemented with MPPT Algorithm for DC Microgrid System,"

Journal of Operation and Automation in Power Engineering, vol. 11, no. 3, pp. 213–222, 2023.
4. R. B. Gonzatti, Y. Li, M. Amirabadi, B. Lehman, and F. Z. Peng, "An Overview of Converter Topologies and Their Derivations and Interrelationships," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 6, pp. 6417–6429, 2022.
5. R. Faraji, L. Ding, T. Rahimi, and M. Kheshti, "Application of soft-switching cell with inherent redundancy properties for enhancing the reliability of boost-based DC–DC converters," IEEE Transactions on Power Electronics, vol. 36, no. 11, pp. 12342–12354, 2021.
6. H. Shayeghi, R. Mohajery, and N. Bizon, "Optimal Design of a Hybrid Controller for DC-DC Buck Converter," in 2023 15th International Conference on Electronics, Computers and Artificial Intelligence (ECAI), 2023: IEEE, pp. 1–6.
7. M. E. Azizkandi, F. Sedaghati, H. Shayeghi, and F. Blaabjerg, "A high voltage gain DC–DC converter based on three winding coupled inductor and voltage multiplier cell," IEEE Transactions on Power Electronics, vol. 35, no. 5, pp. 4558–4567, 2019.
8. H. Ardi, A. Ajami, and M. Sabahi, "A novel high step-up DC–DC converter with continuous input current integrating coupled inductor for renewable energy applications," IEEE transactions on industrial electronics, vol. 65, no. 2, pp. 1306–1315, 2017.
9. J. D. Navamani, A. Lavanya, D. Almakhles, and M. J. Sathik, "A review on segregation of various high gain converter configurations for distributed energy sources," Alexandria Engineering Journal, vol. 61, no. 1, pp. 675–700, 2022.
10. H. Tarzamni, H. S. Gohari, M. Sabahi, and J. Kyyrä, "Non-isolated high step-up dc-dc converters: comparative review and metrics applicability," IEEE Transactions on Power Electronics, 2023.
11. Y. Guan, Y. Cheng, T. Yao, Y. Wang, W. Wang, and D. Xu, "A High-Performance DC–DC Converter with Soft Switching Characteristic and High Voltage Gain," IEEE Transactions on Power Electronics, vol. 37, no. 10, pp. 12279–12288, 2022.
12. L. Qin et al., "Transformer-Less Soft-Switching High-Gain PWM Boost Converter with Reduced Components and Increased Effective Duty Cycle," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 11, no. 2, pp. 1913–1928, 2022.
13. C. Li, H. Li, N. Wang, X. Sun, and L. Cheng, "A Full Soft-Switching High Step-Up DC/DC Converter with Active-Switched-Inductor and Three-Winding Coupled Inductor," IEEE Transactions on Power Electronics, 2023.
14. M. Zamani, A. Aghaie, A. Zamani, R. Tari, M. Abarzadeh, and S. H. Hosseini, "Design and Implementation of Nonisolated High Step-Up DC-DC Converter," International Transactions on Electrical Energy Systems, vol. 2023, 2023.
15. M. Vesali, "A new three winding coupled inductors high step?up DC–DC converter with low input current ripple," IET Power Electronics, 2023.
16. R. Asgarniya and E. Afjei, "A novel high?efficient step?up converter with continuous input current, common ground, and minimum stress on semiconductors," IET Power Electronics, pp. 1-18, 2023.
17. J. Narayanaswamy and S. Mandava, "Non-Isolated Multiport Converter for Renewable Energy Sources: A Comprehensive Review," Energies, vol. 16, no. 4, p. 1834, 2023.
18. X. Fan, H. Sun, Z. Yuan, Z. Li, R. Shi, and N. Ghadimi, "High voltage gain DC/DC converter using coupled inductor and VM techniques," IEEE Access, vol. 8, pp. 131975–131987, 2020.
19. H. Shayeghi, R. Mohajery, N. Bizon, P. Thounthong, and N. Takorabet, "Implementation of PD-PI Controller for Boost Converter Using GWO Algorithm," in 2022 14th International Conference on Electronics, Computers and Artificial Intelligence (ECAI), 2022: IEEE, pp. 1–7.
20. R. Mohajery, H. Shayeghi, and J. L. Villanueva, "PSO-TVAC Based Optimized FOPID Controller for Cascaded DC-DC Boost Converter," International Journal on Technical and Physical Problems of Engineering (IJTPE), vol. 13, pp. 139–146, 2021.
21. M. Veerachary and M. R. Khuntia, "Design and analysis of two-switch-based enhanced gain buck–boost converters," IEEE Transactions on Industrial Electronics, vol. 69, no. 4, pp. 3577–3587, 2021.
22. M. Hosseinpour, M. Ahmadi, A. Seifi, and S. R. Mousavi?Aghdam, "A new transformerless semi?quadratic buck–boost converter based on combination of Cuk and traditional buck–boost converters," International Journal of Circuit Theory and Applications, vol. 50, no. 11, pp. 3926–3948, 2022.
23. N. Genc and Y. Koc, "Experimental verification of an improved soft-switching cascade boost converter," Electric Power Systems Research, vol. 149, pp. 1–9, 2017.
24. S.A. Ansari and J.S. Moghani, "A novel high voltage gain noncoupled inductor SEPIC converter", IEEE Transactions on Industrial Electronics, vol. 66, no. 9. pp.7099–7108, 2019.
25. P.K. Maroti, S. Padmanaban, J.B. Holm-Nielsen, M.S. Bhaskar, M. Meraj, and A. Iqbal, "A new structure of high voltage gain SEPIC converter for renewable energy applications", IEEE Access, vol. 7, pp.89857–89868, 2019.
26. F. M. Shahir, E. Babaei, and M. Farsadi, "Extended topology for a boost DC–DC converter," IEEE Transactions on Power Electronics, vol. 34, no. 3, pp. 2375–2384, 2018.
27. F. M. Shahir, E. Babaei, and M. Farsadi, "A new structure for non-isolated boost dc–dc converter," Journal of Circuits, Systems and Computers, vol. 26, no. 01, p. 1750012, 2017.
28. B. P. Baddipadiga and M. Ferdowsi, "A high-voltage-gain dc-dc converter based on modified dickson charge pump voltage multiplier," IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7707–7715, 2016.
29. B. Zhu, S. Chen, Y. Zhang, and Y. Huang, "An interleaved zero-voltage zero-current switching high step-up DC-DC converter," IEEE Access, vol. 9, pp. 5563–5572, 2020.