A novel single-phase multi-level inverter topology based on bridge-type connected sources with enhanced number of levels per number of devices

FATEMEH ESMAEILI[1] **AND KAZEM VARESI**[1,*]

[1] *Faculty of Electrical Engineering, Power Electronics Research Lab. (PERL), Sahand University of Technology, Tabriz, Iran*
[*] *Corresponding author: k.varesi@sut.ac.ir*

Manuscript received 12 October, 2019; revised 24 January, 2020, accepted 24 January, 2020. Paper no. JEMT-1910-1200.

This paper proposes a developed basic Multi-Level Inverter (MLI) topology that is commercially suited for higher number of levels. The suggested topology can produce larger ratios of steps per DC sources, switches, gate-driver circuits and total devices than recently presented similar structures. The increased levels of suggested topology has led to low Total Harmonic Distortion (THD) and better power quality. Accordingly, the output-side filter can be removed or its size can be reduced. Also, the proposed topology doesn't employ an H-bridge to produce negative levels. So, the total voltage stress on switches is reduced in great extent. All the aforementioned properties make the suggested topology a compact, light and cheaper structure. Also, the suitability for supplying resistive-inductive (*R*-*L*) loads is another merit of suggested topology. Since the magnitude of DC sources influences the number of levels, three different scenarios have been considered for selecting magnitude of DC sources in basic topology. Then, the switching states, key parameters and blocking voltage on switches of suggested basic topology have been presented for each scenario. In the following, the generalized topology have been proposed that is consisted of cascaded basic units. Then, a generalized methodology has been suggested for selecting magnitude of DC sources in generalized topology to minimize redundant switching states and maximize number of voltage levels. To verify properties of suggested topology, it has been compared with similar novel structures. Also, to check correct performance of suggested topology, its basic version has been simulated in PSCAD/EMTDC software. The comparison and simulation outcomes certify advantages and correct operation of proposed topology.

keywords: *Multi-level inverter, Number of levels/devices, Total harmonic distortion, Voltage stress.*

http://dx.doi.org/10.22109/jemt.2020.203960.1200

NOMENCLATURE

N_{Source} Number of DC sources
N_{Switch} Number of switches
N_{IGBT} Number of IGBTs
N_{Driver} Number of gate-driver circuits
N_{Level} Number of voltage levels
N_{Device} Number of total devices
$N_{Variety}$ Variety of DC sources
$V_{o,max}$ Maximum output voltage
VS Voltage stress
TVS Total voltage stress

1. INTRODUCTION

The conventional two-level inverters suffer from high Total Harmonic Distortion (THD) and low power quality issues, which necessitates employment of a bulky filter at the end-side [1]. Also, at medium or high power applications, the semiconductors are imposed to high voltage stress that leads to increased cost and loss and reduced efficiency. The aforementioned problems have been resolved by the advent of Multi-Level Inverters (MLIs) [2]. Simple structure, reduced output voltage THD, high power quality, low EMI, low *dv/dt* and low voltage stress on devices are the main merits that have increased popularity of MLIs [3, 4]. In recent decades, various MLI structures have been presented in the literature that can be categorized into 3 groups: Cascaded MLIs (CMLIs), Diode-Clamped MLIs (DCMLIs) and Flying Capacitor MLIs (FCMLIs) [5–9]. This work concentrates

only on DCMLIs. The CMLIs are formed by DC sources and semiconductors. Many sources and semiconductors are required to produce high levels, which leads to increased cost, weight, size and losses of converter. But, the effect of DC sources on size and cost of MLIs is much more than semiconductors. So, the reduction of DC sources is one of the main objectives of presented MLI structures. The number of semiconductors (switches or diodes) and gate-driver circuits are also important factors that directly influences the size/cost of inverter. Note that the unidirectional and common-emitter bidirectional switches require only one gate-driver circuit, where non-common-emitter bidirectional switches need two gate-driver circuits. Thus, another main design purpose of CMLIs is to produce maximum levels by means of minimum switching devices. A new 35-level developed H-bridge based inverter has been presented in [10] that benefits from large ratio of number of steps per number of sources and switches, but the high voltage stress on S_u and S_d switches is its main shortcoming. A new reduced-source switched-capacitor based CMLI topology with voltage boosting capability has been presented in [11]. Similar to [10], the large voltage stress on S_u and S_d switches is considered is its big disadvantage. The [12–14] have presented extendable basic units for CMLIs that require an H-bridge to produce negative steps. So, the maximum output voltage is imposed to switches of H-bridge, which increases the total voltage stress of converter. The large number of bidirectional switches (IGBTs) and sources required at extended versions, is another drawback of [12–14]. Two symmetrical compact 7 and 13-level CMLIs with decreased conducting switches have been presented in [15]. The large number of bidirectional switches (IGBTs), driver circuits and sources required for increased levels are disadvantage of [15]. Another basic unit has been presented in [16] that requires an H-bridge to generate zero and negative levels. Consequently, the total voltage stress of converter is increased. Another 13-level basic inverter (called "envelope type") with reduced voltage stress on switches has been presented in [17]. The low ratio of levels to sources as well as large number of devices on current flow path are disadvantages of [17]. A 21-level basic topology has been presented in [18]. The topologies presented in [17, 18] can produce negative levels without an end-side H-bridge. So, the total voltage stress is decreased. The large voltage stresses on switches and numerous devices on current path are disadvantages of [18].

This paper suggests a modified basic topology (derived from [19]) that produces higher maximum output voltage and larger ratio of steps per devices (sources, switches, gate drivers) than [19]. The proposed basic topology can produce negative and zero levels without an end-side H-bridge. This reduces the total voltage stress of converter. The suggested basic units can be cascaded to achieve more steps. Also, the suggested topology can efficiently supply the resistive-inductive (*R-L*) loads. In the following, the suggested basic topology is introduced and its operational modes and switching states for three different sets of DC sources are illustrated. The extended version of suggested basic topology is investigated in Section 3. The comparative analysis and modulation technique are presented in Sections 4 and 5. The simulation outcomes are given in Section 6. The conclusions are presented in Section 7.

2. PROPOSED BASIC TOPOLOGY

A. Topology of basic topology

The suggested basic topology (shown in Fig. 1b) has been derived from topology presented in [19] (shown in Fig. 1a).

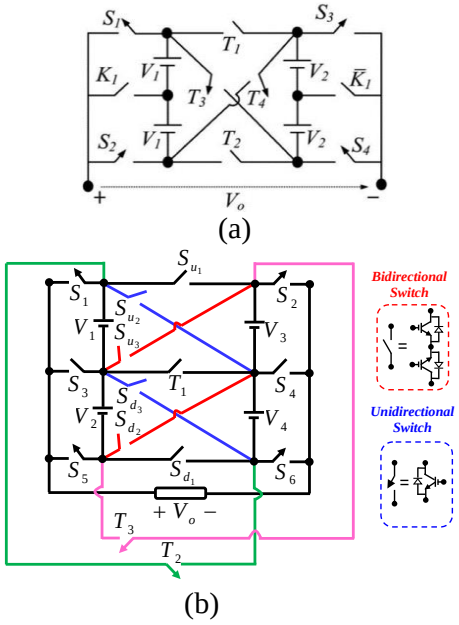

Fig. 1. (a) 25-level topology presented in [19], (b) Proposed basic topology.

The topology of [19] produces 25 voltage levels by means of 4 DC sources, 4 bidirectional and 6 unidirectional switches. In order to produce negative, zero and positive levels, the DC sources on each leg of [19] must be identical. This increases the redundant states and decreases distinct voltage steps. This problem has been resolved in proposed topology by adding only 5 switches, where the amplitude of DC sources can be freely selected such that maximum possible (distinct) voltage levels be achieved. The suggested basic unit is formed by 4 DC sources (the same as [19]) and 15 power switches. The S_1, S_2, S_5, S_6, T_2, and T_3 switches are unidirectional (realized by an IGBT and an antiparallel diode) and the others are bidirectional switches (two series-connected common-emitter IGBTs with antiparallel diodes). Since the common-emitter bidirectional switches require only one gate driver circuit, the total demanded driver count (N_{Driver}) of suggested basic unit is the same as switch count (N_{Switch}). The total component count (defined as $N_{Source} + N_{Switch} + N_{Driver}$) is equal to $N_{Device} = 34$. So:

$$N_{Source} = 4,\ N_{Switch} = 15,\ N_{Driver} = 15,\ N_{Device} = 34 \quad \textbf{(1)}$$

B. Operation of basic topology

The number of levels of MLIs is depended on the magnitude of input DC sources. In this subsection, the operation of proposed topology during three different scenarios and sets of DC sources is investigated.

B.1. Symmetric form (P_1)

This scenario is known as "Symmetric" version, where the size of input sources are the same ($V_1 = V_2 = V_3 = V_4 = V_{dc}$). Table 1 illustrates switching scheme of proposed basic symmetric unit.

As seen from Table 1, the proposed symmetric basic topology has 79 switching states but only 9 of them lead to distinct voltage levels of 0, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$ and $\pm 4V_{dc}$ ($N_{Level} = 9$). The other remaining 70 switching states are all redundant. Also, the

maximum producible output voltage is $V_{o,max} = 4V_{dc}$. Since all the input DC sources are the same, the variety number of sources is 1.

$$\begin{aligned} V_{o,\max,P_1} &= 4V_{dc},\ N_{Variety,P_1} = 1 \\ N_{Level,P_1} &= 2(V_{o,\max,P_1}/V_{dc}) + 1 = 9 \end{aligned} \tag{2}$$

Please note that the variety of DC sources is equal to number of distinct (unique) amplitudes that have been considered for DC sources.

The Voltage Stress (VS) and Normalized Voltage Stress (NVS) on switches of suggested basic structure during first scenario (P_1) have been shown in Table 2. It is observed that only 2 switches (T_2, T_3) have VS of $V_{o,max}$, the VS on other switches is much less than $V_{o,max}$. Note that, high VSs increases expense and losses of switches and decreases efficiency of converter. The Average of Normalized Voltage Stresses ($ANVS$) on switches is about 56.7%, which is almost half of $V_{o,max}$.

B.2. First asymmetric form (P_2)

In this Scenario, the amplitude of input sources are supposed to be $V_3 = V_4 = 2V_1 = 2V_2 = 2V_{dc}$. Table 3 illustrates the switching pattern of proposed basic topology and produced output voltage levels during second scenario.

Table 3 shows that the first asymmetric form of proposed basic topology can produce 13 different voltage levels of $0, \pm V_{dc}, \ldots, \pm 5V_{dc}$ and $\pm 6V_{dc}$ ($N_{Level} = 13$). So, compared with symmetric version, the redundant switching states has decreased from 70 to 66, which still is considerable amount. The peak output voltage is $6V_{dc}$ and variety number of DC sources is 2.

$$\begin{aligned} V_{o,\max,P_2} &= 6V_{dc},\ N_{Variety,P_2} = 2 \\ N_{Level,P_2} &= 2(V_{o,\max,P_2}/V_{dc}) + 1 = 13 \end{aligned} \tag{3}$$

The VS on switches of proposed basic topology in second scenario have been shown in Table 4. As evident from Table 4, the VS on T_2, T_3 switches is $V_{o,max}$ and the this amount for other switches is less than $V_{o,max}$. The least NVS is about 16.67% that belongs to S_3 switch. Also, the $ANVS$ is about 60%, which is slightly higher than that of symmetric version (P_1).

B.3. Second asymmetric form (P_3)

As presented in Sub-sections B.1 and B.2, there exists numerous redundant switching states in first and second scenarios. In third scenario, the size of input sources are chosen as (4) to reduce redundant states and increase number of diverse steps.

$$V_1 = V_{dc},\ V_2 = 2V_{dc},\ V_3 = 7V_{dc},\ V_4 = 14V_{dc} \tag{4}$$

The switching pattern of proposed basic topology in such situation (P_3) has been shown in Table 5. As seen, the suggested basic unit produces 49 unique voltage levels of $0, \pm V_{dc}, \ldots, \pm 23V_{dc}$ and $\pm 24V_{dc}$ ($N_{Level} = 49$) by applying third scenario. The maximum output voltage and also the variety number of input sources are respectively $24V_{dc}$ and 4 as (5).

$$\begin{cases} V_{o,\max,P_3} = 24V_{dc},\ N_{Variety,P_3} = 4 \\ N_{Level,P_3} = 2(V_{o,\max,P_3}/V_{dc}) + 1 = 49 \end{cases} \tag{5}$$

The VS and also the NVS on switches of proposed basic unit in third scenario have been shown in Table 6. Similar to 1^{st} and 2^{nd} scenarios, the VS of T_2, T_3 switches is $V_{o,max}$. But, the VS of other switches are much less than $V_{o,max}$. The least NVS belongs to S_3, which is about 8.3%. The $ANVS$ of proposed basic unit in third scenario is about 68% that is higher than that of 1^{st} and 2^{nd} scenarios.

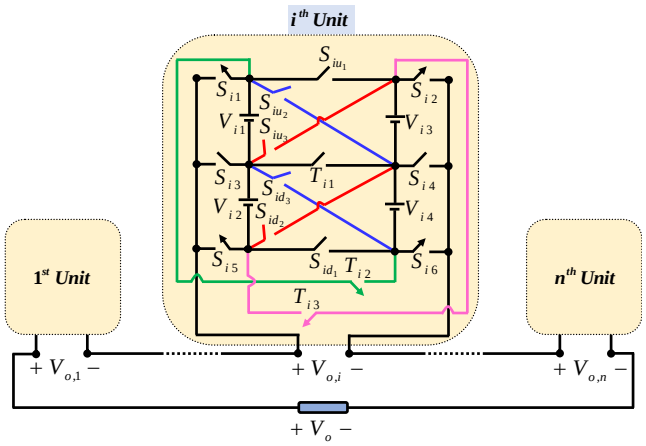

Fig. 2. Proposed cascaded topology.

3. PROPOSED CASCADED TOPOLOGY

A. Topology

The proposed extended topology with increased number of levels can be realized by cascading suggested basic units, as shown in Fig. 2. The proposed cascaded topology is consisted of $4n$ input DC sources, $15n$ switches and $15n$ gate driver circuits, as presented in (6). The number of required unidirectional and bidirectional switches are $9n$ and $6n$, respectively. The total number of required devices of proposed cascaded topology is $N_{Device} = 34n$.

$$N_{Source} = 4n,\ N_{Switch} = N_{Driver} = 15n,\ N_{Device} = 34n \tag{6}$$

B. Decision on magnitude of DC sources

As mentioned in Section 2, the number of levels in MLIs directly depends on magnitude of DC sources. This section proposes an algorithm for choosing the size of DC sources in suggested cascaded topology, by which the redundant states are reduced and number of steps are increased. The V_{i1}, V_{i2}, V_{i3} and V_{i4} represent the input DC sources of cascaded i^{th} unit. Note that the size of each DC source is equal to maximum producible voltage of previous sources plus V_{dc}, as (7).

$$\begin{cases} V_{11} = V_{dc},\ V_{12} = 2V_{dc},\ V_{13} = 7V_{dc},\ V_{14} = 14V_{dc} \\ V_{j1} \overset{(j=2,\cdots,n)}{=} \left(\sum_{i=1}^{j-1} \left(\frac{V_{o,\max_i}}{V_{dc}} \right) + 1 \right) V_{dc} \\ V_{j2} = 2V_{j1},\ V_{j3} = 7V_{j1},\ V_{j4} = 14V_{j1} \end{cases} \tag{7}$$

By simplifying (7), the magnitude of input DC sources of i^{th} unit can be achieved as (8).

$$\begin{cases} V_{i1} = 25^{(i-1)}V_{dc},\ V_{i2} = 2 \times 25^{(i-1)}V_{dc} \\ V_{i3} = 7 \times 25^{(i-1)}V_{dc},\ V_{i4} = 14 \times 25^{(i-1)}V_{dc} \end{cases} \tag{8}$$

Table 2. Voltage Stress (VS) on switches of proposed symmetric basic topology (P_1)

Switch	VS	NVS [%]	Switch	VS	NVS [%]
S_1	$V_1+V_2=2V_{dc}$	50	S_{u3}	$V_1+V_3+V_4=3V_{dc}$	75
S_2	$V_4+V_3=2V_{dc}$	50	S_{d1}	$V_3+V_4=2V_{dc}$	50
S_3	$V_2=V_{dc}$	25	S_{d2}	$V_1+V_2+V_4=3V_{dc}$	75
S_4	$V_4=V_{dc}$	25	S_{d3}	$V_2+V_3+V_4=3V_{dc}$	75
S_5	$V_1+V_2=2V_{dc}$	50	T_1	$V_1+V_4=2V_{dc}$	50
S_6	$V_4+V_3=2V_{dc}$	50	T_2	$V_1+V_2+V_3+V_4=4V_{dc}$	100
S_{u1}	$V_4+V_3=2V_{dc}$	50	T_3	$V_1+V_2+V_3+V_4=4V_{dc}$	100
S_{u2}	$V_4=V_{dc}$	25			
Average of $VSs=\frac{\sum VS_{S,T}}{N_{switch}}$		2.267 V_{dc}	Average of $NVSs=\frac{\sum VS_{S,T}}{N_{switch}\times V_{o,\max}}$		56.67%

Table 4. Voltage Stress (VS) on switches of proposed basic topology in second scenario (P_2)

Switch	VS	NVS [%]	Switch	VS	NVS [%]
S_1	$V_1+V_2=2V_{dc}$	33.33	S_{u3}	$V_1+V_3+V_4=5V_{dc}$	83.33
S_2	$V_4+V_3=4V_{dc}$	66.67	S_{d1}	$V_3+V_4=4V_{dc}$	66.67
S_3	$V_2=V_{dc}$	16.67	S_{d2}	$V_1+V_2+V_4=4V_{dc}$	66.67
S_4	$V_4=2V_{dc}$	33.33	S_{d3}	$V_2+V_3+V_4=5V_{dc}$	83.33
S_5	$V_1+V_2=2V_{dc}$	33.33	T_1	$V_1+V_4=3V_{dc}$	50
S_6	$V_4+V_3=4V_{dc}$	66.67	T_2	$V_1+V_2+V_3+V_4=6V_{dc}$	100
S_{u1}	$V_4+V_3=4V_{dc}$	66.67	T_3	$V_1+V_2+V_3+V_4=6V_{dc}$	100
S_{u2}	$V_4=2V_{dc}$	33.33			
Average of $VSs=\frac{\sum VS_{S,T}}{N_{switch}}$		$3.6V_{dc}$	Average of $NVSs=\frac{\sum VS_{S,T}}{N_{switch}\times V_{o,\max}}$		60%

Table 6. Voltage Stress (VS) on switches of proposed basic topology in second scenario (P_3)

Switch	VS	NVS [%]	Switch	VS	NVS [%]
S_1	$V_1+V_2=3V_{dc}$	12.50	S_{u3}	$V_1+V_3+V_4=22V_{dc}$	58.33
S_2	$V_4+V_3=21V_{dc}$	87.5	S_{d1}	$V_3+V_4=21V_{dc}$	87.5
S_3	$V_2=2V_{dc}$	8.33	S_{d2}	$V_1+V_2+V_4=17V_{dc}$	70.83
S_4	$V_4=14V_{dc}$	58.33	S_{d3}	$V_2+V_3+V_4=23V_{dc}$	95.83
S_5	$V_1+V_2=3V_{dc}$	12.5	T_1	$V_1+V_4=15V_{dc}$	62.5
S_6	$V_4+V_3=21V_{dc}$	87.5	T_2	$V_1+V_2+V_3+V_4=24V_{dc}$	100
S_{u1}	$V_4+V_3=21V_{dc}$	87.5	T_3	$V_1+V_2+V_3+V_4=24V_{dc}$	100
S_{u2}	$V_4=14V_{dc}$	58.33			
Average of $VSs=\frac{\sum VS_{S,T}}{N_{switch}}$		$16.33V_{dc}$	Average of $NVSs=\frac{\sum VS_{S,T}}{N_{switch}\times V_{o,\max}}$		68%

Also, V_{o,max_i} represents peak output voltage of i^{th} unit that can be obtained from (9).

$$V_{o,\max_i}=V_{i1}+V_{i2}+V_{i3}+V_{i4}=24\times 25^{(i-1)}V_{dc} \quad \textbf{(9)}$$

The maximum output voltage and also the number of steps of suggested structure with n cascaded units can be computed respectively from (10) and (11). The (10) and (11) confirm that the maximum output voltage and number of levels of proposed cascaded topology dramatically increase by increment of cascaded units (n). For example, the maximum output voltage and number of levels of suggested extended topology with only two cascaded units (n=2) are considerable amounts of $V_{o,max}=624V_{dc}$ and $N_{Level}=1249$, respectively.

$$V_{o,\max}=\sum_{i=1}^{n}V_{o,\max_i}=(25^n-1)V_{dc} \quad \textbf{(10)}$$

$$N_{Level}=2(V_{o,\max}/V_{dc})+1=(2\times 25^n)-1 \quad \textbf{(11)}$$

The variety of DC sources in proposed cascaded topology is $N_{Variety}=4n$.

C. Voltage stress calculations

The VS on switches of suggested cascaded converter is investigated in this subsection. It is observed from Tables 2, 4, and 6 that the VS on switches of suggested basic unit are as (12):

$$\begin{aligned}
&VS_{S_{i1}}=VS_{S_{i5}}=(V_{i1}+V_{i2})\\
&VS_{S_{i2}}=VS_{S_{i6}}=VS_{S_{iu1}}=VS_{S_{id1}}=(V_{i3}+V_{i4})\\
&VS_{S_{i3}}=(V_{i2}),\ VS_{S_{i4}}=VS_{S_{iu2}}=(V_{i4})\\
&VS_{S_{iu3}}=(V_{i1}+V_{i3}+V_{i4}),\ VS_{S_{id2}}=(V_{i1}+V_{i2}+V_{i4})\\
&VS_{S_{id3}}=(V_{i2}+V_{i3}+V_{i4}),\ VS_{T_{i1}}=(V_{i1}+V_{i4})\\
&VS_{T_{i2}}=VS_{T_{i3}}=(V_{i1}+V_{i2}+V_{i3}+V_{i4})
\end{aligned} \quad \textbf{(12)}$$

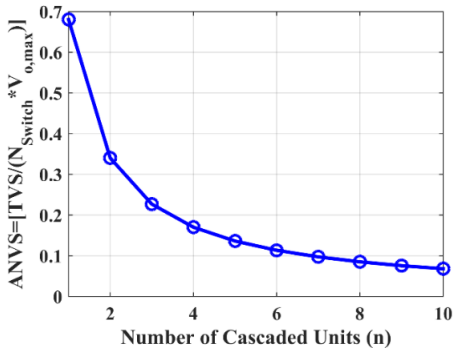

Fig. 3. ANVS of suggested cascaded topology for various number of cascaded units (n).

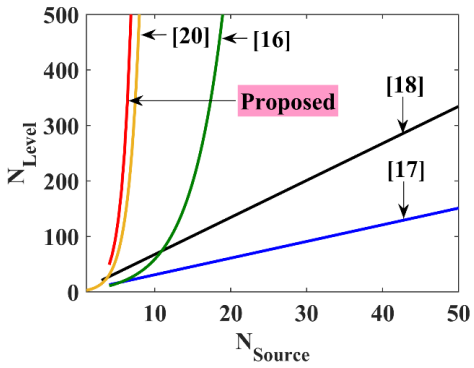

Fig. 4. Number of levels versus number of sources.

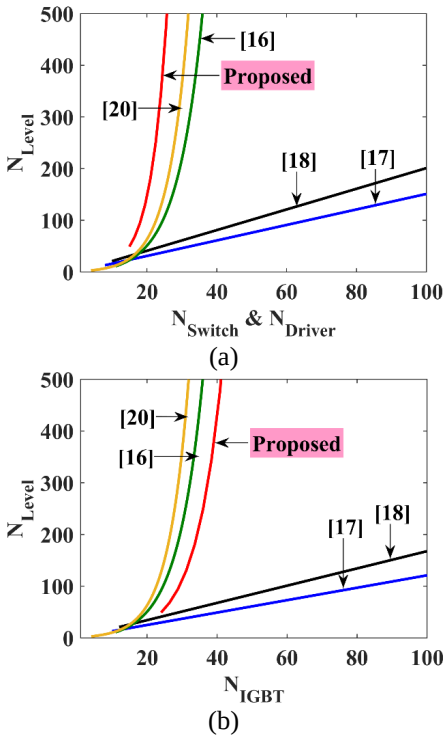

Fig. 5. Number of levels versus number of (a) Switches (or driver circuits); (b) IGBTs.

So, the Total Voltage Stress (TVS) on switches of unit i can be obtained by (13):

$$\begin{aligned} TVS_i &= \sum VS_{S_i,T_i,S_{u_i},S_{d_i}} \\ &= (7V_{i1} + 7V_{i2} + 8V_{i3} + 12V_{i4}) \end{aligned} \quad \textbf{(13)}$$

The TVS of proposed cascaded topology (with n cascaded unit) can be achieved by replacing (8) in (13) and summing up the TVS of cascaded units ($TVSi$), as (14):

$$TVS = \sum_{i=1}^{n} TVS_i = \frac{245}{24}(25^n - 1)V_{dc} \quad \textbf{(14)}$$

The $ANVS$ of suggested cascaded topology can be calculated from (15):

$$\begin{aligned} ANVS &= \left[\sum_{i=1}^{n} VS_i / \left(N_{Switch} \times V_{o,\max}\right)\right] \\ &= [49/(72n)] \end{aligned} \quad \textbf{(15)}$$

The $ANVS$ of suggested cascaded topology (with n cascaded units) has been illustrated in Fig. 3. This figure shows that the $ANVS$ of suggested topology is always less than 70%. Also, it is observed that by increment of cascaded units (n), the $ANVS$ of suggested converter dramatically decreases. For example, the $ANVS$ of suggested converter with 4 cascaded units is less than 20%.

4. COMPARISON RESULTS

To validate superiority of suggested cascaded topology over other similar structures, it has been compared with [16–18] and conventional Cascaded H-Bridge (CHB) inverter [20]. The comparisons have been done from viewpoints of number of DC sources (N_{Source}), switches (N_{Switch}), IGBTs (N_{IGBT}), gate driver circuits (N_{Driver}), total devices (N_{Device}), number of levels (N_{Level}), variety of DC sources ($N_{Variety}$), maximum output voltage ($V_{o,max}$) and Total Voltage Stress (TVS). The comparison outcomes have been shown in Table 7 and Figs. 4-9. Based on Fig. 4, the suggested topology produces larger steps per DC sources than [16–18, 20]. In other words, at equal-level versions, the suggested topology utilizes less DC sources than [[16–18, 20]. Thus, the proposed converter will be cheaper, lighter and more compact than [16–18, 20]. Also, Fig. 4 indicates that with the same number of sources, the suggested topology can produce more levels than [16–18, 20]. According to Fig. 5a, the suggested structure requires less switches and gate driver circuits than [16–18, 20] to generate equal number of levels, which leads to simple, small and cheaper structure and easy control strategy. The proposed topology utilizes several bidirectional switches, realized by two IGBTs. Then, the number of required IGBTs has also been investigated in Fig. 5b. This figure shows that at equal-level versions, the proposed topology requires more IGBTs than [16, 20]. From this point of view, the suggested converter has better condition than [17, 18]. Fig. 5b indicates that the suggested structure can produce more steps than [17, 18] with equal IGBTs. According to Fig. 6, with the same number of devices, the suggested topology generates more levels than [16–18, 20], which leads to less THD and accordingly reduced-size output filter. Also, the suggested structure requires fewer devices than other structures to produce equal number of levels. This property results in a reduction in size, weight and expense

Table 7. Comparison results

Topology	[16]	[17]	[18]	CHB	Proposed (Cascaded)
N_{Source}	$3n+1$	$4n$	$3n$	n	$4n$
N_{Switch}	$5n+6$	$8n$	$10n$	$4n$	$15n$
N_{IGBT}	$5n+6$	$10n$	$12n$	$4n$	$24n$
N_{Driver}	$5n+6$	$8n$	$10n$	$4n$	$15n$
N_{Level}	$2^{(n+3)}-5$	$12n+1$	$20n+1$	$2^{(n+1)}-1$	$2(25)^n-1$
N_{Device}	13n+13	$20n$	$23n$	$9n$	$34n$
$N_{Variety}$	$3n+1$	2	3	n	$4n$
$V_{o,max}/V_{dc}$	$2^{(n+3)}-3$	$6n$	$10n$	2^n-1	$(25)^n-1$
TVS/V_{dc}	$7(2^{(n+2)})-22$	$20n$	$44n$	$4[2^n-1]$	$\left(\frac{245}{24}\right)[(25)^n-1]$

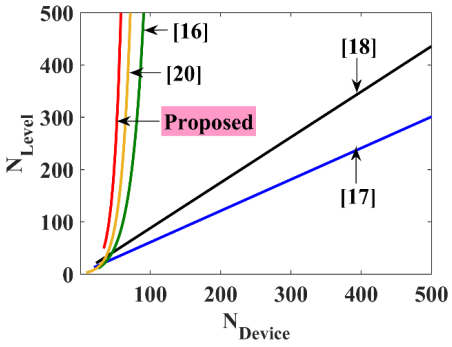

Fig. 6. Number of levels versus number of total devices.

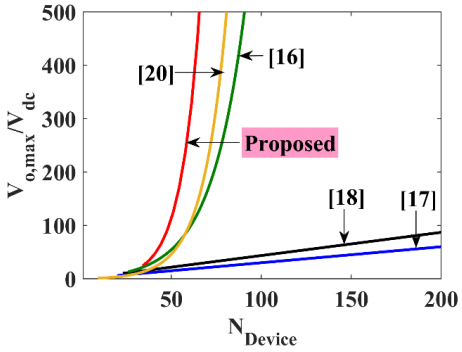

Fig. 7. Peak output voltage versus number of total devices.

of converter.

Fig. 7 shows maximum output voltage ($V_{o,max}$) versus number of devices. Based on Fig. 7, the proposed converter uses fewer components than [16–18, 20] to generate desired output power (or$V_{o,max}$), which reduces volume and expense of proposed converter. Similar to Fig. 6, by employing equal count of components, the proposed structure generates higher $V_{o,max}$ (and consequently higher output powers) than [16–18, 20], which is an important advantage.

Fig. 8 shows that for different number of cascaded units, the *ANVS* of proposed converter is higher than [16–18], which is the main drawback of suggested topology. It must be note that the size, cost and loss of switches are increased by increment of *ANVS*. From this point of view, the [20] has worst condition. It is evident from Fig. 8 that the *ANVS* of suggested structure is always less than 70%.It is also observed that by increment of cascaded units (n), the *ANVS* of suggested topology dramatically decreases. For n>5, the *ANVS* of proposed topology is around 10%, which is small enough and acceptable. The variety of DC sources influences the total cost of converter. Higher varieties lead to increased cost. According to Table 7 and Fig. 9, the least varieties belong to [17, 18] with 2 and 3 sets of sources, respectively. Also it is observed that the ($N_{Level}/N_{Variety}$) of suggested converter is higher than [16, 20].

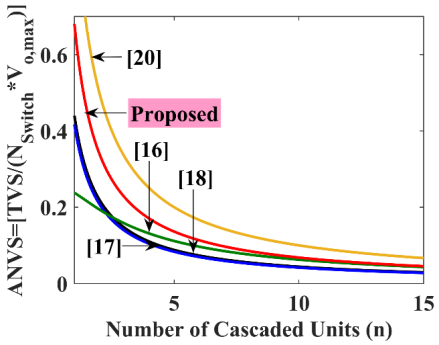

Fig. 8. ANVS on switches versus number of cascaded units (n).

5. NEAREST LEVEL MODULATION STRATEGY

In this paper, the nearest level or so called "fundamental frequency" strategy has been employed for producing switching pulses. In this method, the reference waveform (with fundamental frequency of 50[Hz] and maximum amplitude of peak positive level) is compared with producible voltage steps. Then, the closest step to reference is produced. Note that the desired voltage levels are produced based on the switching tables presented in Section 2. The ratio of amplitude of reference waveform to peak positive level is called modulation index. The difference between reference and producible voltage levels (called "error") for both positive and negative half cycles has been shown in Fig. 10. It is seen that when the error reaches to its top value (0.5), the level changes.

6. SIMULATION RESULTS

To evaluate correct operation of suggested structure, it has been simulated in PSCAD/EMTDC. The parameter values used in

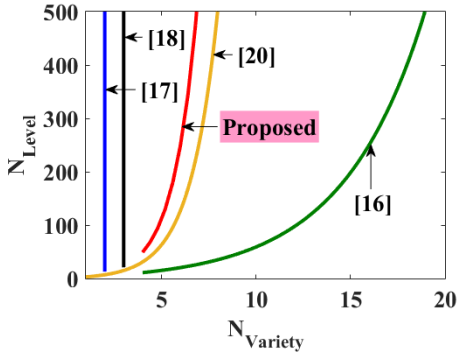

Fig. 9. Number of levels versus variety number of DC sources.

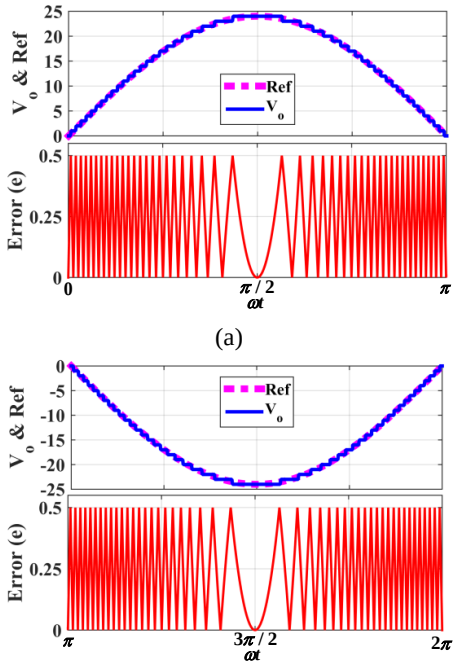

Fig. 10. Nearest level modulation technique, (a) Positive, (b) Negative, half cycle.

simulations for previously stated 3 scenarios have been presented in Table 8.

Table 8. Simulation parameters

Scenario	DC sources V_1, V_2, V_3, V_4	Load (R,L)	Modulation index (m)	Fundamental frequency (f)
1^{st} (P_1)	10[V],10[V], 10[V],10[V]	40[Ω], 0.1[H]	0.98	50[Hz]
2^{nd} (P_2)	10[V],10[V], 20[V],20[V]	60[Ω], 0.15[H]		
3^{rd} (P_3)	10[V],20[V], 70[V],140[V]	240[Ω], 0.6[H]		

Fig. 11 shows the produced voltage and load current waveforms of suggested converter during aforementioned 3 scenarios. It is observed from Fig. 11a-11c that the proposed topology can produce 9, 13 and 49 voltage levels respectively in 1^{st}, 2^{nd}, and 3^{rd} scenarios, which are confirmed by (2), (3), and (5). The max-

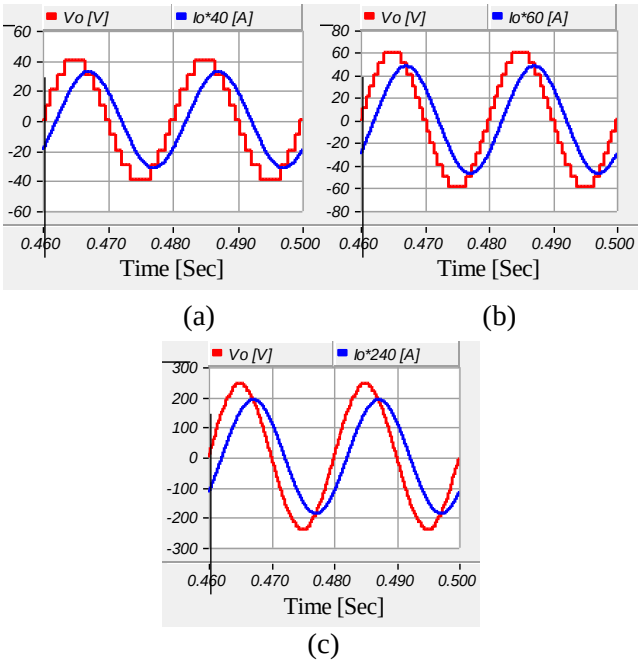

Fig. 11. Load voltage and current waveform of proposed topology during: (a) 1^{st}, (b) 2^{nd}, (c) 3^{rd}, scenario.

imum output voltages ($V_{o,max}$) of proposed topology during $1^{st} - 3^{rd}$ scenarios are respectively about 40[V], 60[V] and 240[V]. The obtained values are confirmed respectively by (2), (3), and (5). Also, the load peak currents ($I_{o,max}$) during $1^{st} - 3^{rd}$ scenarios are respectively about 0.8[A], 0.79[A] and 0.79[A]. Please note that for better view, the load current waveforms in $1^{st} - 3^{rd}$ scenarios, have been shown with magnifying factors of 40, 60 and 240, respectively.

Also, due to the resistive-inductive (R-L) nature of load, the phase difference of 38° is observed between load voltage and current waveforms that is validated by $\Delta\varphi = arctan(L\omega/R)$. So, the proposed topology can efficiently supply the R-L load types. The THD of suggested topology (taking 127 harmonic orders into consideration) in $1^{st} - 3^{rd}$ scenarios, are respectively about 8.98%, 5.97%, and 1.17%. It is observed that as the number of levels increases, the quality of output voltage of proposed topology is improved. Since the THD of proposed topology is small, there exists no need to filter at the load side.

To evaluate dynamic response of suggested topology, it has been simulated during sudden step-up and step-down load changes. It has been considered that during first mode ($0 \leq t < 0.4[Sec]$), the resistive load ($R_1 = R$) is the same as Table 8. But, at t=0.4[Sec] (second mode $0.4 \leq t < 0.5[Sec]$) it becomes doubled ($R_2 = 2R$), and finally at t=0.5[Sec] (third mode $0.5 \leq t < 0.6[Sec]$) it changes to half ($R_3 = R/2$). Fig. 12 shows the dynamic load change results of proposed topology during $1^{st} - 3^{rd}$ scenarios.

It is evident from Fig. 12 that the proposed topology has kept its normal operation during sudden step-up (t=0.4[Sec]) and step-down (t=0.5[Sec]) load changes. As seen, the current of proposed topology has been decreased by increment of resistive load (R) in second mode and has been increased by decrement of R in third mode. However, during these load changes, the number of steps and the magnitude of Vo has not changed, which confirms suitable dynamic performance of proposed topology.

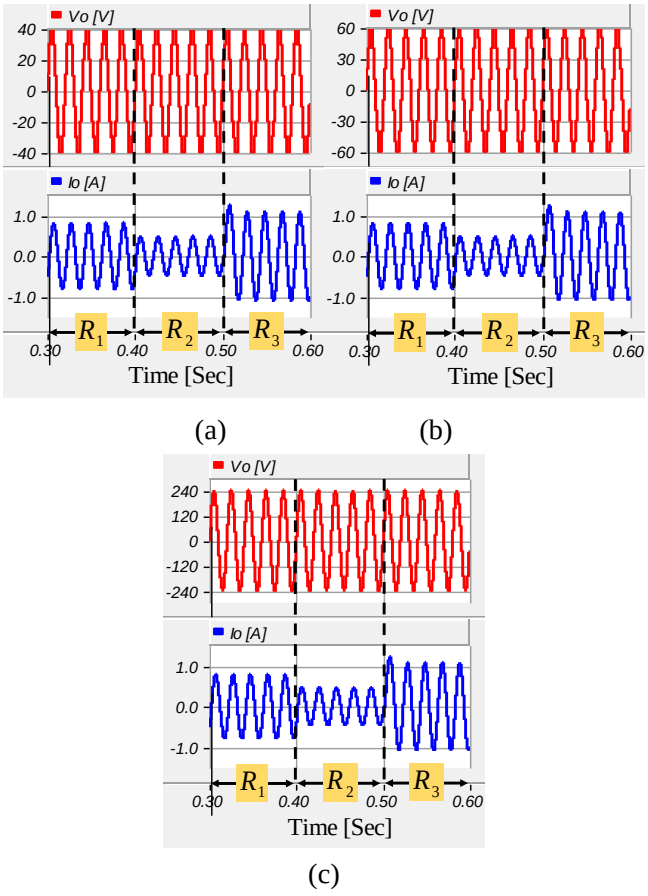

Fig. 12. Dynamic performance of proposed topology during: (a) 1^{st}, (b) 2^{nd}, (c) 3^{rd}, scenario [$R_1 = (R_2/2) = 2R_3 = R$].

Normally, the expense and losses of switches are decided by their voltage and current stress. Since the highest voltage stresses (worst case) happen in 3^{rd} scenario, only this scenario is considered during voltage/current stress investigations. The voltage waveform on switches of proposed topology (in 3^{rd} scenario) have been illustrated in Fig. 13.

Fig. 13 indicates that the voltage stress on switches of proposed topology (in 3^{rd} scenario) are: VS_{S1}=30[V], VS_{S2}=210[V], VS_{S3}=20[V], VS_{S4}=140[V], VS_{S5}=30[V], VS_{S6}=210[V], VS_{Su1}=210[V], VS_{Su2}=140[V], VS_{Su3}=220[V], VS_{Sd1}=210[V], VS_{Sd2}=170[V], VS_{Sd3}=230[V], VS_{T1}=150[V], VS_{T2}=240[V], VS_{T3}=240[V]. As confirmed by Table 6, the highest voltage stress among switches belongs to T_2 and T_3 switches, which is equal to $V_{o,max}$. The other switches experience less voltages than $V_{o,max}$.

In the proposed topology, the load current passes through the switches. Consequently, the current stress of switches (peak current) is the same as maximum load current ($I_{o,max}$). The current waveform flowing through the switches of proposed topology have been shown in Fig. 14. It is observed that the current stress of switches is equal to peak load current, which is about $I_{o,max} = 0.79[A]$.

The efficiency of proposed topology (during 3^{rd} scenario) versus different load (R) values has been indicated in Fig. 15.

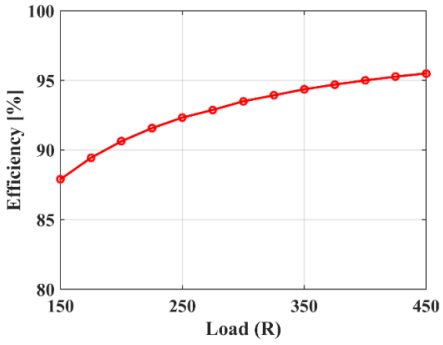

Fig. 15. Efficiency of proposed topology (3^{rd} scenario) versus different load (R) values.

This figure validates that the efficiency of suggested structure stays over 87% in wide range of load values. Note that in efficiency analysis, the on-state resistances of unidirectional and bidirectional switches (realized by MOSFETs) have been assumed to be 0.55 Ω and 1.1 Ω, respectively.

7. CONCLUSION

This study has suggested a new single-phase basic 49-level inverter topology that benefits from simple structure, easy control strategy, low voltage stress on switches, low THD and increased number of steps per devices. Then, the operational modes and switching states of suggested basic topology have been explained for three different algorithms of selecting magnitude of DC sources. The suggested basic topology can be extended by cascading basic units, which increases the number of levels. Accordingly, the THD of suggested cascaded topology is reduced and its quality is improved. Therefore, the end-side filter can be removed or downsized. The comparison results certify that with the same count of devices, the suggested topology can produce more levels than others. In other words, the suggested topology employs less devices than others to generate the same count of levels. The reduction in number of devices leads to reduced weight, size, cost and complexity of suggested converter. Also, the suggested topology can efficiently supply the low power factor (R-L) loads. The comparison and simulation outcomes prove the advantages and correct performance of suggested topology during steady-state and load-change (dynamic) conditions.

REFERENCES

1. M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson, "A General Review of Multilevel Inverters Based on Main Submodules: Structural Point of View," IEEE Transactions on Power Electronics, vol. 34, no. 10, pp. 9479-9502, 2019.
2. A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," IEEE Transactions on Power Electronics, vol. 30, pp. 18-36, 2015.
3. A. A. Gandomi, S. Saeidabadi, S. H. Hosseini, E. Babaei, and Y. A. Gandomi, "Flexible transformer-based multilevel inverter topologies," IET Power Electronics, vol. 12, pp. 578-587, 2018.
4. F. Esmaeili and K. Varesi, "A Modified Single-Phase Multi-Level Inverter with Increased Number of Steps," Iranian Conference on Renewable Energy & Distributed Generation (ICREDG), Tehran, Iran, 2019.
5. K. K. Gupta and P. Bhatnagar, "Multilevel inverters: conventional and emerging topologies and their control," Academic Press, 2017.

6. S. S. Lee, "Single-Stage Switched-Capacitor Module (S 3 CM) Topology for Cascaded Multilevel Inverter," IEEE Transactions on Power Electronics, vol. 33, pp. 8204-8207, 2018.
7. S. Shi, X. Wang, S. Zheng, Y. Zhang, and D. Lu, "A New Diode-Clamped Multilevel Inverter with Balance Voltages of DC Capacitors," IEEE Transactions on Energy Conversion, vol. 33, no. 4, pp. 2220-2228, 2018.
8. A. A. Gandomi, S. Saeidabadi, and S. H. Hosseini, "A high step up flying capacitor inverter with the voltage balancing control method," Power Electronics, Drive Systems & Technologies Conference (PEDSTC), pp. 55-60, 2017.
9. A. A. Gandomi, K. Varesi, and S. H. Hosseini, "Control strategy applied on double flying capacitor multi-cell inverter for increasing number of generated voltage levels," IET Power Electronics, vol. 8, pp. 887-897, 2015.
10. K. Varesi, M. Karimi, and P. Kargar, "A New Cascaded 35-Level Inverter with Reduced Switch Count," Iranian Conference on Renewable Energy & Distributed Generation (ICREDG), Tehran, Iran, 2019.
11. K. Varesi, M. Karimi, and P. Kargar, "A new basic step-up cascaded 35-level topology extendable to higher number of levels," Power Electronics, Drives Systems and Technologies Conference (PEDSTC), pp. 1-6, 2019.
12. R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Reduction of Power Electronic Elements in Multilevel Converters Using a New Cascade Structure," IEEE Transactions on Industrial Electronics, vol. 62, pp. 256-269, 2015.
13. S. H. Hosseini, K. Varesi, J. F. Ardashir, A. A. Gandomi, and S. Saeidabadi, "An attempt to improve output voltage quality of developed multilevel inverter topology by increasing the number of levels," International Conference on Electrical and Electronics Engineering (ELECO), pp. 665-669, 2015.
14. E. Babaei, C. Buccella, and C. Cecati, "New 8-Level Basic Structure for Cascaded Multilevel Inverters with Reduced Number of Switches and DC Voltage Sources," Journal of Circuits, Systems and Computers, vol. 28, p. 1950038, 2019.
15. S. S. Lee, M. Sidorov, N. R. N. Idris, and Y. E. Heng, "A Symmetrical Cascaded Compact-Module Multilevel Inverter (CCM-MLI) With Pulsewidth Modulation," IEEE Transactions on Industrial Electronics, vol. 65, pp. 4631-4639, 2018.
16. E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," IEEE Transactions on Industrial Electronics, vol. 62, pp. 922-929, 2015.
17. E. Samadaei, S. Gholamian, A. Sheikholeslami, and J. Adabi, "An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters With Reduced Components," IEEE Transactions on Industrial Electronics, vol. 63, no. 11, pp. 7148-7156, 2016.
18. S. Sabyasachi, V. B. Borghate, and S. K. Maddugari, "A 21-Level Bipolar Single-Phase Modular Multilevel Inverter," Journal of Circuits, Systems and Computers, 2019.
19. R. S. Alishah, S. H. Hosseini, E. Babaei, M. Sabahi, and A. Z. Gharehkoushan, "Optimal design of new cascade multilevel converter topology based on series connection of extended sub-multilevel units," IET Power Electronics, vol. 9, no. 7, pp. 1341-1349, 2016.
20. E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," Energy Conversion and Management, vol. 50, pp. 2761-2767, 2009.

Table 1. Switching of proposed symmetric basic topology (P_1)

No.	$S_1S_2S_3S_4S_5S_6S_{u1}S_{u2}S_{u3}S_{d1}S_{d2}S_{d3}T_1T_2T_3$	Vo	
1	000011000100000	0	0
2	100001000000010		
3	001001000001000		
4	000110000010000		
5	100100001000000		
6	001100000000100		
7	010010000000001		
8	011000001000000		
9	110000100000000		
10	110000000000100	$+(V_1-V_3)$	
11	001100100000000	$-(V_1-V_3)$	
12	100100000001000	$+(V_1-V_4)$	
13	001001010000000	$-(V_1-V_4)$	
14	011000000010000	$+(V_2-V_3)$	
15	000110001000000	$-(V_2-V_3)$	
16	001100000100000	$+(V_2-V_4)$	
17	000011000000100	$-(V_2-V_4)$	
18	110000000100000	$+(V_1+V_2-V_3-V_4)$	
19	000011100000000	$-(V_1+V_2-V_3-V_4)$	
20	100100000000100	$+V_1$	$+V_{dc}$
21	100001000001000		
22	110000001000000		
23	001001000100000	$+V_2$	
24	011000000000001		
25	001100000010000		
26	100100100000000	$+V_3$	
27	001100001000000		
28	100001010000000	$+V_4$	
29	000011000010000		
30	001001000000000		
31	110000000010000	$+(V_1+V_2-V_3)$	
32	100100000100000	$+(V_1+V_2-V_4)$	
33	001001100000000	$-(V_1-V_3-V_4)$	
34	000011001000000	$-(V_2-V_3-V_4)$	
35	011000100000000	$-V_1$	$-V_{dc}$
36	001001000000010		
37	001100010000000		
38	000110000000100	$-V_2$	
39	000011000001000		
40	010010001000000		
41	010010000010000	$-V_3$	
42	011000000000100		
43	110000010000000		
44	000110000100000	$-V_4$	
45	001100000001000		
46	000110100000000	$-(V_1+V_2-V_3)$	
47	000011010000000	$-(V_1+V_2-V_4)$	
48	110000000001000	$+(V_1-V_3-V_4)$	
49	011000000100000	$+(V_2-V_3-V_4)$	
50	100001000100000	$+(V_1+V_2)$	$+2V_{dc}$
51	100100000010000		
52	110000000000001		
53	100001100000000	$+(V_3+V_4)$	
54	001001001000000		
55	000011000000001		
56	100100001000000	$+(V_1+V_3)$	
57	100001000000100	$+(V_1+V_4)$	
58	001100000000001	$+(V_2+V_3)$	
59	001001000010000	$+(V_2+V_4)$	
60	010010100000000	$-(V_1+V_2)$	$-2V_{dc}$
61	000110001000000		
62	000011000000010		
63	010010000100000	$-(V_3+V_4)$	
64	110000000000010		
65	011000000001000		
66	011000010000000	$-(V_1+V_3)$	
67	001100000000010	$-(V_1+V_4)$	
68	010010000000100	$-(V_2+V_3)$	
69	000110000001000	$-(V_2+V_3)$	
70	100100000000001	$+(V_1+V_2+V_3)$	$+3V_{dc}$
71	100001000010000	$+(V_1+V_2+V_4)$	
72	100001001000000	$+(V_1+V_3+V_4)$	
73	001001000000001	$+(V_2+V_3+V_4)$	
74	010010010000000	$-(V_1+V_2+V_3)$	$-3V_{dc}$
75	000110000000010	$-(V_1+V_2+V_4)$	
76	011000000000010	$-(V_2+V_3+V_4)$	
77	010010000001000	$-(V_1+V_2+V_3)$	
78	100001000000001	$+(V_1+V_2+V_3+V_4)$	$+4V_{dc}$
79	010010000000010	$-(V_1+V_2+V_3+V_4)$	$-4V_{dc}$

Table 3. Switching of proposed basic topology in 2^{nd} scenario

No.	$S_1S_2S_3S_4S_5S_6S_{u1}S_{u2}S_{u3}S_{d1}S_{d2}S_{d3}T_1T_2T_3$	Vo	
1	000011000100000	0	0
2	100001000000010		
3	001001000001000		
4	000110000010000		
5	100100001000000		
6	001100000000100		
7	010010000000001		
8	011000001000000		
9	110000100000000		
10	110000000010000	$+(V_1+V_2-V_3)$	
11	000110100000000	$-(V_1+V_2-V_3)$	
12	100100000100000	$+(V_1+V_2-V_4)$	
13	000011010000000	$-(V_1+V_2-V_4)$	
14	100100000000100	$+V_1$	$+V_{dc}$
15	100001000001000		
16	110000001000000		
17	001001000100000	$+V_2$	
18	011000000000001		
19	001100000010000		
20	001100100000000	$-(V_1-V_3)$	
21	001001010000000	$-(V_1-V_4)$	
22	000110001000000	$-(V_2-V_3)$	
23	000011000000100	$-(V_2-V_4)$	
24	001100100000000	$-V_1$	$-V_{dc}$
25	001001000000010		
26	001100010000000		
27	000110000000100	$-V_2$	
28	000011000001000		
29	010010001000000		
30	110000000000100	$+(V_1-V_3)$	
31	100100000001000	$+(V_1-V_4)$	
32	011000000010000	$+(V_2-V_3)$	
33	001100000100000	$+(V_2-V_4)$	
34	100100100000000	$+V_3$	$+2V_{dc}$
35	001100001000000		
36	100001010000000	$+V_4$	
37	000011000010000		
38	001001000000000		
39	100001000100000	$+(V_1+V_2)$	
40	100100000010000		
41	110000000000001		
42	000011100000000	$-(V_1+V_2-V_3-V_4)$	
43	010010000010000	$-V_3$	$-2V_{dc}$
44	011000000000100		
45	110000010000000	$-V_4$	
46	000110000100000		
47	001100000001000		
48	010010100000000	$-(V_1+V_2)$	
49	000110001000000		
50	000011000000010		
51	110000000100000	$+(V_1+V_2-V_3-V_4)$	
52	100100001000000	$+(V_1+V_3)$	$+3V_{dc}$
53	100001000000100	$+(V_1+V_4)$	
54	001100000000001	$+(V_2+V_3)$	
55	001001000010000	$+(V_2+V_4)$	
56	001001100000000	$-(V_1-V_3-V_4)$	
57	000011001000000	$-(V_2-V_3-V_4)$	
58	011000010000000	$-(V_1+V_3)$	$-3V_{dc}$
59	001100000000010	$-(V_1+V_4)$	
60	010010000000100	$-(V_2+V_3)$	
61	000110000001000	$-(V_2+V_4)$	
62	110000000001000	$+(V_1-V_3-V_4)$	
63	011000000100000	$+(V_2-V_3-V_4)$	
64	100001100000000	$+(V_3+V_4)$	$+4V_{dc}$
65	001001001000000		
66	000011000000001		
67	100100000000001	$+(V_1+V_2+V_3)$	
68	100001000010000	$+(V_1+V_2+V_4)$	
69	010010000100000	$-(V_3+V_4)$	$-4V_{dc}$
70	110000000000010		
71	011000000001000		
72	010010010000000	$-(V_1+V_2+V_3)$	
73	000110000000010	$-(V_1+V_2+V_4)$	
74	100001001000000	$+(V_1+V_3+V_4)$	$+5V_{dc}$
75	001001000000001	$+(V_2+V_3+V_4)$	
76	011000000000010	$-(V_1+V_3+V_4)$	$-5V_{dc}$
77	010010000001000	$-(V_2+V_3+V_4)$	
78	100001000000001	$+(V_1+V_2+V_3+V_4)$	$+6V_{dc}$
79	010010000000010	$-(V_1+V_2+V_3+V_4)$	$-6V_{dc}$

Table 5. Switching of proposed basic topology in 3^{rd} scenario

No.	$S_1S_2S_3S_4S_5S_6S_{u1}S_{u2}S_{u3}S_{d1}S_{d2}S_{d3}T_1T_2T_3$	Vo	
1	000011000100000	0	0
2	100001000000010		
3	001001000001000		
4	000110000010000		
5	100100001000000		
6	001100000000100		
7	010010000000001		
8	011000001000000		
9	110000100000000		
10	100100000000100	$+V_1$	$+V_{dc}$
11	100001000001000		
12	110000001000000		
13	011000100000000	$-V_1$	$-V_{dc}$
14	001001000000010		
15	001100010000000		
16	001001000100000	$+V_2$	$+2V_{dc}$
17	011000000000001		
18	001100000010000		
19	000110000000100	$-V_2$	$-2V_{dc}$
20	000011000001000		
21	010010001000000		
22	100001000100000	$+(V_1+V_2)$	$+3V_{dc}$
23	100100000010000		
24	110000000000001		
25	010010100000000	$-(V_1+V_2)$	$-3V_{dc}$
26	000110001000000		
27	000011000000010		
28	000110100000000	$-(V_1+V_2-V_3)$	$+4V_{dc}$
29	110000000010000	$+(V_1+V_2-V_3)$	$-4V_{dc}$
30	000110001000000	$-(V_2-V_3)$	$+5V_{dc}$
31	011000000010000	$+(V_2-V_3)$	$-5V_{dc}$
32	001100100000000	$-(V_1-V_3)$	$+6V_{dc}$
33	110000000000100	$+(V_1-V_3)$	$-6V_{dc}$
34	100100100000000	$+V_3$	$+7V_{dc}$
35	001100001000000		
36	010010000010000	$-V_3$	$+7V_{dc}$
37	011000000000100		
38	110000010000000		
39	100100001000000	$+(V_1+V_3)$	$+8V_{dc}$
40	011000010000000	$-(V_1+V_3)$	$-8V_{dc}$
41	001100000000001	$+(V_2+V_3)$	$+9V_{dc}$
42	010010000000100	$-(V_2+V_3)$	$-9V_{dc}$
43	100100000000001	$+(V_1+V_2+V_3)$	$+10V_{dc}$
44	010010010000000	$-(V_1+V_2+V_3)$	$-10V_{dc}$
45	000011010000000	$-(V_1+V_2-V_4)$	$+11V_{dc}$
46	100100000100000	$+(V_1+V_2-V_4)$	$-11V_{dc}$
47	000011000000100	$-(V_2-V_4)$	$+12V_{dc}$
48	001100000100000	$+(V_2-V_4)$	$-12V_{dc}$
49	001001010000000	$-(V_1-V_4)$	$+13V_{dc}$
50	100100000001000	$+(V_1-V_4)$	$-13V_{dc}$
51	100001010000000	$+V_4$	$+14V_{dc}$
52	000011000010000		
53	001001000000000		
54	000110000100000	$-V_4$	$-14V_{dc}$
55	001100000001000		
56	100001000000100	$+(V_1+V_4)$	$+15V_{dc}$
57	001100000000010	$-(V_1+V_4)$	$-15V_{dc}$
58	001001000010000	$+(V_2+V_4)$	$+16V_{dc}$
59	000110000001000	$-(V_2+V_4)$	$-16V_{dc}$
60	100001000010000	$+(V_1+V_2+V_4)$	$+17V_{dc}$
61	000110000000010	$-(V_1+V_2+V_4)$	$-17V_{dc}$
62	000011100000000	$-(V_1+V_2-V_3-V_4)$	$+18V_{dc}$
63	110000000100000	$+(V_1+V_2-V_3-V_4)$	$-18V_{dc}$
64	000011001000000	$-(V_2-V_3-V_4)$	$+19V_{dc}$
65	011000000100000	$+(V_2-V_3-V_4)$	$-19V_{dc}$
66	001001100000000	$-(V_1-V_3-V_4)$	$+20V_{dc}$
67	110000000001000	$+(V_1-V_3-V_4)$	$-20V_{dc}$
68	100001100000000	$+(V_3+V_4)$	$+21V_{dc}$
69	001001001000000		
70	000011000000001		
71	010010000100000	$-(V_3+V_4)$	$-21V_{dc}$
72	110000000000010		
73	011000000001000		
74	100001001000000	$+(V_1+V_3+V_4)$	$+22V_{dc}$
75	011000000000010	$-(V_1+V_3+V_4)$	$-22V_{dc}$
76	001001000000001	$+(V_2+V_3+V_4)$	$+23V_{dc}$
77	010010000001000	$-(V_2+V_3+V_4)$	$-23V_{dc}$
78	100001000000001	$+(V_1+V_2+V_3+V_4)$	$+24V_{dc}$
79	010010000000010	$-(V_1+V_2+V_3+V_4)$	$-24V_{dc}$

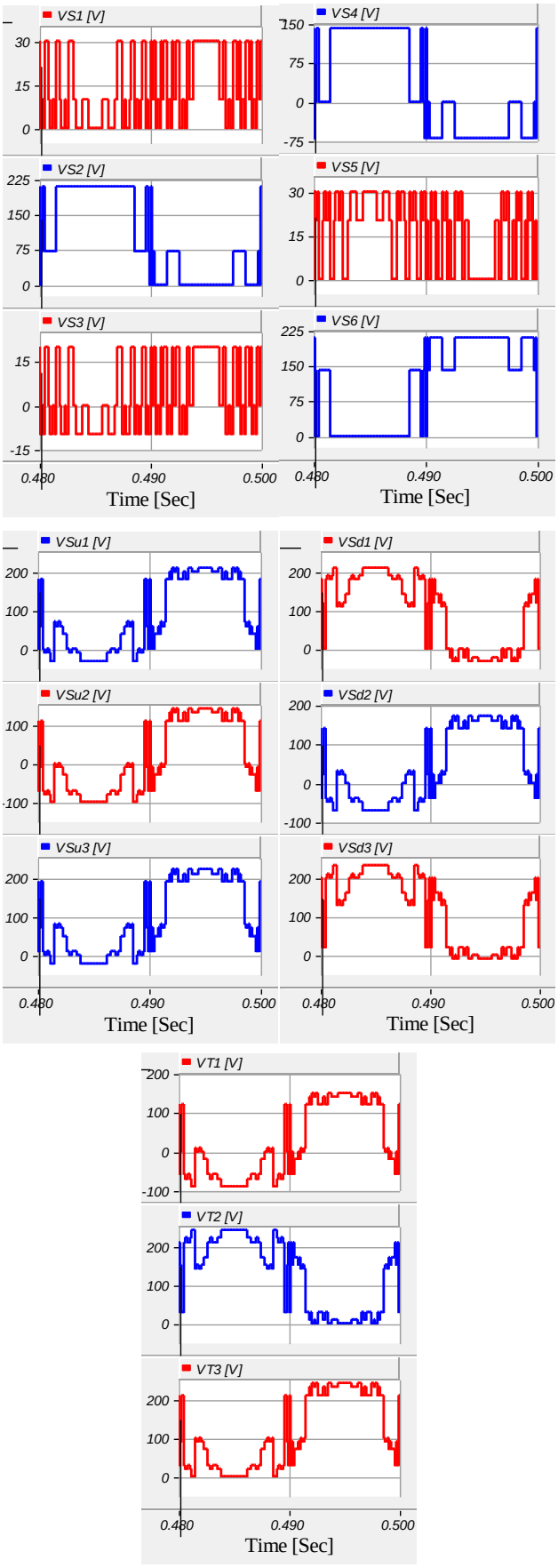

Fig. 13. Voltage waveform (stress) of switches of proposed topology during 3rd scenario.

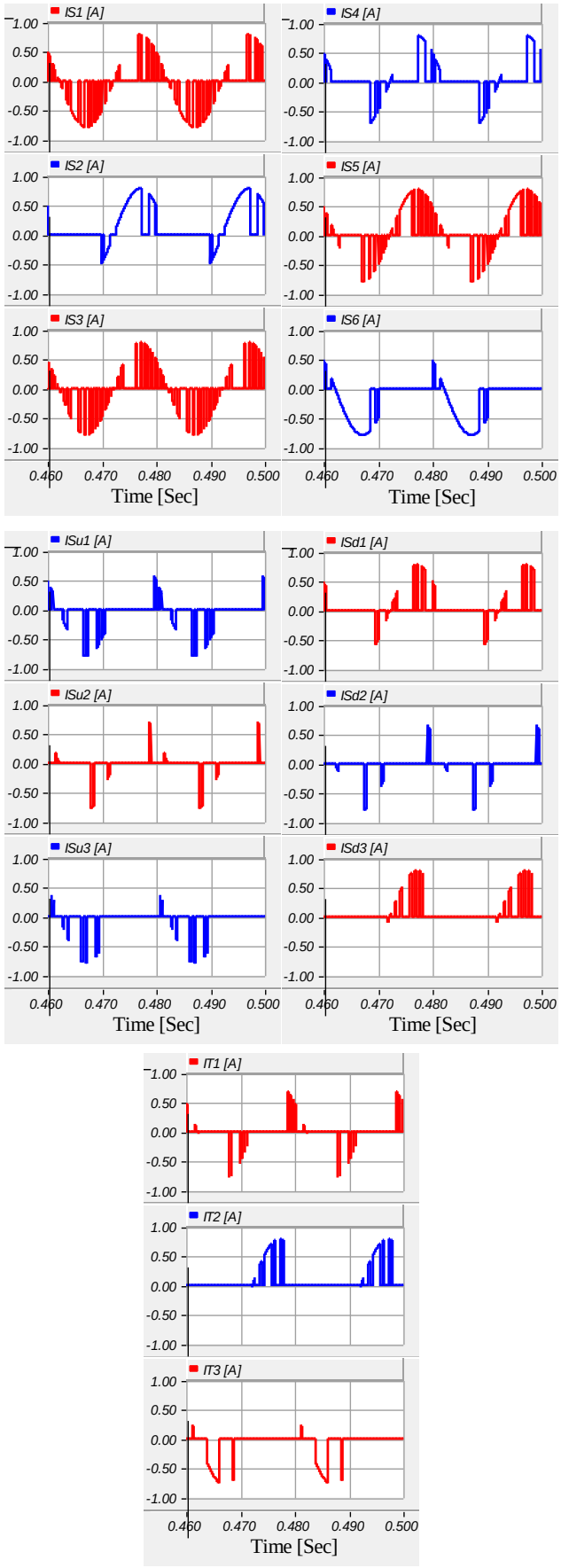

Fig. 14. Current waveform (stress) of switches of proposed topology during 3rd scenario.