Presenting a new structure for interlinking converter in hybrid AC-DC microgrids to improve voltage quality

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In this paper, a new structure is presented for interlinking converter (IC) to improve voltage in hybrid AC-DC microgrids. This structure consists of series IC (SIC) and a parallel IC (PIC) parts. The PIC is responsible for exchanging the power between sub-grids and decreasing voltage unbalance indices. Based on the free capacity of PIC, voltage unbalance compensation reference is calculated on the AC sub-grid side. In the series part of IC, any kind of voltage disturbance is compensated for the sensitive load. In order to increase the speed of dynamic response and to decrease the loss in SIC, the resistor of output filter is removed and then, fluctuations are damped in an active way in the control system. This is carried out through feeding back the current of the capacitor of the output filter and applying it to the control system, and using the current mode control in inner loop which improves the stability. Proportional-resonant and proportional-differential controllers are used in the control part of SIC. Therefore, proper tracking of the reference signal is guaranteed. Results obtained from the simulation of the case study system in MATLAB software verify the capabilities of the proposed approach.

keywords: *Hybrid AC-DC microgrid, Interlinking converter, Power quality, Unbalance compensation, Voltage sag, Active damping.*

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1. INTRODUCTION

Remarkable benefits such as lack of reactive power, higher efficiency, no skin effect on lines, no need for synchronization, etc. are among the numerous advantages of DC distribution networks over AC distribution networks. However, the considerable expansion and development of AC distribution networks over the last century makes it unlikely to swiftly substitute them with their DC counterparts. So, an economic yet practical solution to take advantage of DC distribution networks will be incorporating hybrid AC-DC microgrids in current AC networks. As mentioned in various references, hybrid AC-DC microgrids are considered as the main parts of future smart distribution networks. On the other hand, the substantial increase of sensitive loads (e.g. huge data centers) requires enhanced power quality and reliability indicators. In the absence of such improvements, the consumer may incur significant costs [1].

A hybrid AC-DC microgrid is composed of three main parts: AC sub-grid, DC sub-grid, and IC converter [2]. Depending on the conditions of a microgrid, different functions can be considered for an IC. For example in [3, 4], IC converter has been used for regulating the DC sub-grid voltage. Whereas, in [5, 6], it has been used to transfer power between two sub-grids. In [7], a battery has been used as a power and voltage regulator in IC structure. In [8], LTCL structure has been used in the output of IC. This has been done to improve the quality of load voltage and network current. However, due to the high order of the case study system, and the large number of measured parameters, the probability of instability is high.

Improving power quality indices is one of the most attractive topics in AC microgrids [1]. References related to this field include those that use power quality improving devices such as APF [9] and those that use an interfacing converter between DG and network to improve power quality indices. It is worth noting that, the second approach has received more attention since it is more cost-effective.

Interfacing converters can help in two ways to improve power quali-ty indices;

- Each converter behaves like an APF so that in addition to injecting active and reactive power, it can inject harmonic or unbalanced current or voltage into the network [10, 11].
- Interfacing converters existing in the network can improve power quality indices in coordination with each other [12–

14].

In interfacing converters which also play the role of APF, there is a possibility of overload due to existence of different impedances between load and distributed generations. Therefore, using these approaches can only be justified in places where a single energy generating source supplies the entire load. On the other hand, in references focusing on the coordination between interfacing converters, the simplest form of a network i.e. only two distributed generation units and one load has been considered and the focus is on improving voltage quality indices [13, 14].

In another case, a sensitive load has been considered at one of the network buses and then, interfacing converters improve the voltage quality of sensitive load bus by generating harmonic and/or unbalanced voltage [15]. In both cases, the voltage generated by distributed generation sources loses its balanced sinusoidal state. Therefore, the voltage quality is improved at the cost of destroying the voltage quality of all other loads distributed all over the network. However, this paper proposes using the whole capacity of existing converters in the network to improve voltage quality. The most available converter in the hybrid AC-DC microgrid is the IC converter which connects the AC and DC sub-grids [16].

In [17, 18], the series converter is used to improve the voltage quality of the hybrid AC-DC microgrid. In these references the series converter is located between the upstream network and the AC sub-grid, so, the entire upstream network current passing through the series converter and the rated power of the series converter is greatly increased. On the other hand, if there is an unbalanced load on the AC sub-grid, the voltage of AC sub-grid will remain unbalanced. In other words, the series converter only improves the disturbances in the upstream network voltage. In [16, 19, 20] IC is used to compensate for the harmonic voltage generated by the nonlinear loads. Although the distribution network usually is a 3ph-4wire system, so far little attention has been paid to power quality problems in this type of network.

In this paper, a new structure is proposed for IC converter to improve power quality indices. The IC converter is divided into two parts: PIC and SIC. This structure differs from the conventional ICs introduced in [7, 21, 22] in three parts; a) using 4-leg converters with the purpose of dealing with zero sequence, b) adding a series converter to compensate for power quality disturbances at critical loads and, c) ability to compensate for voltage unbalance using the free capacity of the PIC converter.

The main duty of PIC is to exchange power between AC and DC sub-grids. Considering the state of loads in hybrid microgrid, it can be concluded that PIC has no load or low load during most hours of the day. Therefore, the capacity of PIC can be used for secondary goals in addition to transferring power between the AC and DC sub-grids. One of the secondary goals is to improve power quality indices, and in this paper decreasing voltage unbalance in AC sub-grid is considered. To achieve this goal, the indices of voltage unbalance, free capacity of PIC (the difference between the rated power of the converter and the power exchanged between two sub-grids), and adaptive virtual impedance are used.

One of the most common power quality phenomena is the voltage sag which cannot be compensated through parallel converters. This phenomenon causes costly problems in sensitive loads [23]. One of the best approaches for preventing the destructive effects of this phenomenon is using a series converter. On the other hand, modifying the transient response when a fault occurs, and removing voltage sag are very important tasks [24, 25]. Using a series resistor with the passive filter of SIC output is one of the ways to damp fluctuations. However, this approach has some disadvantages such as power loss and reduction of the capability of removing switching ripple. Therefore, two different problems are encountered; increasing the resistance causes switching ripples to appear at the output, and decreasing it causes stability margin to reduce. The approach proposed here is to use a virtual resistor. Under such conditions, by applying a feedback from the current of LC passive filter to the control system, a virtual damping is created. This causes the costs of system to decrease, and consequently removes the two aforementioned problems. Briefly, the main contribution of the paper includes:

- voltage unbalance compensation in 3ph-4w network by using the free capacity of IC with no need to unbalanced load current meas-urement,
- Defining an adaptive unbalance reference compensation based on the current flowing through each branch of IC to avoid PIC over-loading,
- Series converter control by multi-loop control including virtual resistor, PD and PR controller as well as extraction of dynamic model of series 4-leg converter, which lead to increased response speed, reduced losses, reduced switching ripple, and precise tracking of voltage reference.

In the following sections, first the structure of the hybrid AC-DC microgrid is investigated and then, a brief discussion is presented about the way the AC and DC sub-grids are controlled. In Section 3, generating reference signals for PIC and SIC is explained. The reference signal of PIC is generated based on the frequency of the AC sub-grid, voltage of DC sub-grid, and voltage unbalance indices in AC sub-grid. Moreover, the reference signal of SIC is generated based on the positive sequence voltage of the point of common coupling (PCC), and the voltage sag detector is implemented based on the positive sequence voltage and its critical value. In Section 4, dynamic modeling of PIC and SIC converters is carried out in order to design the controller. Section 5 presents the simulation results of the system under study in MATLAB software based on several scenarios. Finally, section 6 concludes the paper.

2. STRUCTURE OF THE HYBRID AC-DC MICROGRID

In order to improve a voltage quality index, the series converter can be connected to the hybrid microgrid in four different ways (Fig. 1). Among these four structures shown in Fig. 1, structure (a) is selected for three reasons:

- There is no need to use a DC source for the series converter (In the two structures shown in Fig. 1 (c) and (d), a rectifier must be used to supply the series converter).
- The rated power of the series converter is much lower compared to the structures shown in Fig. 1 (b) and (d).
- In the structure shown in Fig. 1, the power exchange capacity between two sub-grids increases.

The structure of the implemented hybrid microgrid is as shown in Fig. 2. As can be seen in this figure, the AC sub-grid is considered as a three-phase four-wire system. The reasons behind this selection can be attributed to the distribution network topology and the ways the single-phase loads are supplied. PIC is composed of two power converters; a 4-leg inverter and

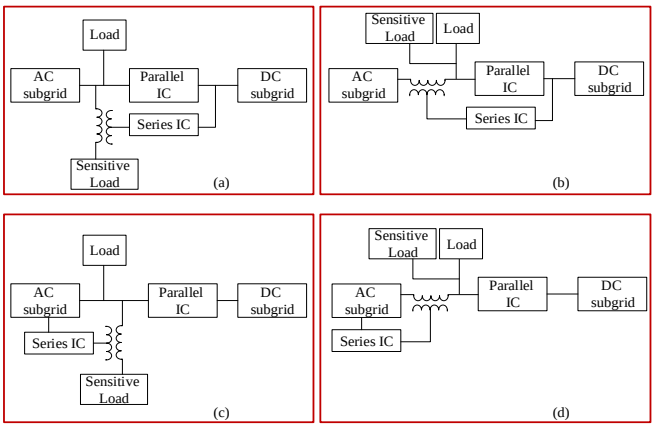

Fig. 1. Different structure through which the series converter can be connected to the hybrid AC-DC microgrid.

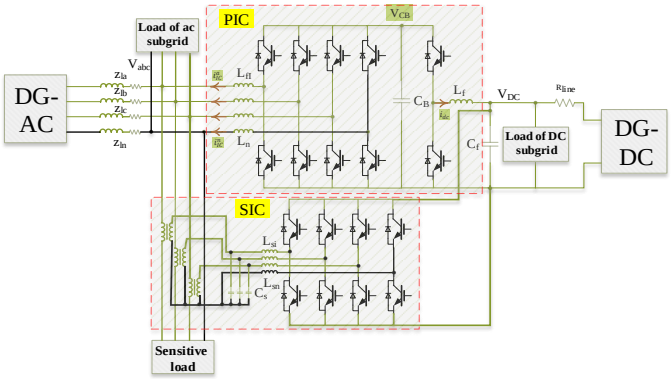

Fig. 2. Structure of the proposed hybrid AC-DC microgrid.

a buck/boost converter. This converter provides the capability of creating a difference in voltage levels in AC and DC sub-grid. It is responsible for stabilizing the voltage of capacitor CB at a predefined value. The SIC converter can be connected to the buck/boost converter. However, increasing the turns ratio of the output transformer can lead to the same result. Therefore, PIC only uses the buck/boost converter.

A. The AC sub-grid

The AC sub-grid is a set of energy generation units and different loads. Therefore, the energy generation units can be controlled based on droop equations presented below [26]:

$$\begin{aligned} \omega_{AC}(i) &= \omega_{AC}^{ref} - m_i \times P_i \\ E(i) &= V_{AC}^{ref} - n_i \times Q_i \end{aligned} \qquad i = 1,2,...,j \tag{1}$$

where ω_{AC} and E are angular frequency reference and the reference voltage of converter respectively. ω_{AC}^{ref} and V_{AC}^{ref} are the angular frequency reference and the reference voltage of sub-grid under no-load conditions, m and n denote the droop coefficients of frequency and voltage of the sub-grid, and P and Q are the output active and reactive power of the converter and finally j is the number of power sources in the AC sub-grid.

According to [27], all energy generation units can be modeled as one single source. Therefore, instead of using several energy generation units, their equivalent circuit model can be used.

B. DC sub-grid

Like the AC sub-grid, all energy generation sources are considered as a single equivalent energy generation source in the DC sub-grid. These sources are controlled using droop control approach [28]:

$$V_{DC}(i) = V_{DC}^{ref} - R_{d(i)} \times i_o(i) \quad i = 1,2,...,k \tag{2}$$

where V_{DC} is the reference voltage of converter, V_{DC}^{ref} is the reference voltage of converter under no-load conditions, R_d is the droop coefficient, io is the output current of the converter, and k is the number of energy generation units located in the DC sub-grid side.

3. GENERATING REFERENCE VOLTAGE AND CURRENT SIGNALS

In the control process of power electronic converters, it is important how to generate reference signals. In this section, the ways the reference current is generated for PIC and the reference voltage is generated for SIC are explained.

A. The reference current of PIC

The PIC converter has two major duties: exchanging power between two sub-grids and decreasing voltage unbalance indices at PCC. The objectives are achieved through injecting or absorbing an amount of current proportional to the power required and voltage unbalance indices.

A.1. Power exchange between two sub-grids

To calculate the amount of power transferred between two sub-grids, it is necessary to measure the frequency of the AC sub-grid and the voltage of DC sub-grid. However, measuring units of these two parameters are not comparable to each other. Therefore, by using Eq. (3) these two indices are converted into values between -1 and 0 [29]:

$$\begin{aligned} f_{pu}^{AC} &= \frac{f - f_{max}}{f_{max} - f_{min}} \\ v_{pu}^{DC} &= \frac{v_{DC} - v_{max}}{v_{max} - v_{min}}. \end{aligned} \tag{3}$$

In these equation, f and v_{DC} are the frequency of the AC sub-grid and the voltage of DC sub-grid, and subscripts *max* and *min* represent the maximum and minimum allowable values of the frequency and voltage, respectively. To decrease the loss, IC will enter the system only under the conditions that the values of f_{pu}^{AC} and v_{pu}^{DC} are less than a certain value. Therefore, a droop equation like (4) and (5) can be used to calculate the power transfer between sub-grids [29]:

$$P_{PICa} = \begin{cases} 0 & 0 < f_{pu}^{AC} \le f_T \\ -k_a\left(f_{pu}^{AC} - f_T\right) & f_B \le f_{pu}^{AC} \le f_T \\ P_T & -1 \le f_{pu}^{AC} < f_B \end{cases}$$
$$P_{PICb} = \begin{cases} 0 & 0 < v_{pu}^{DC} \le v_T \\ -k_b\left(v_{pu}^{DC} - v_T\right) & v_B \le v_{pu}^{DC} \le v_T \\ P_T & -1 \le v_{pu}^{DC} < v_B \end{cases} \tag{4}$$

$$P_{PIC} = P_{PICa} - P_{PICb} \tag{5}$$

In these equations, P_{PICa} and P_{PICb} are the power demanded by the AC and DC sub-grids, P_{PIC} is the actual power transferred

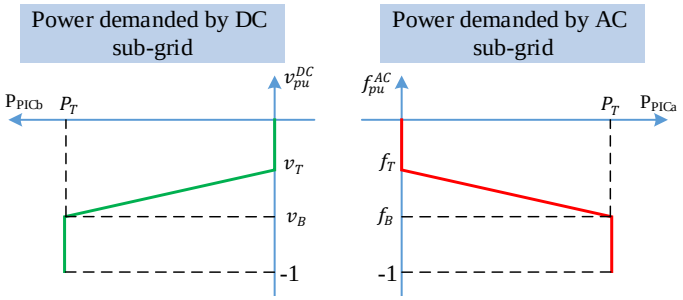

Fig. 3. Droop characteristic curve for calculating the power demanded by the sub-grids.

by PIC and P_T is the maximum transferrable power which is basically limited by the rated power of PIC. In Fig. 3, other parameters of Eq. (4) are shown. Reactive power exchanged by PIC only takes place when the active power is transferred from DC sub-grid side towards AC sub-grid side. The reason for this is described in [30]. Therefore, the reference reactive power is calculated using Eq. (6):

$$Q_{PIC} = \begin{cases} k_q \left(v_e - v_{ac}^n\right) & P_{PIC} \geq 0 \\ 0 & P_{PIC} < 0 \end{cases} \tag{6}$$

$$v_e = \sqrt{\left(v^1\right)^2 + \left(v^2\right)^2 + \frac{\left(v^0\right)^2}{2}} \tag{7}$$

where k_q is the droop slope of voltage control, k_q is the effective voltage of the PIC terminal under voltage unbalance conditions [31], and v_{ac}^n are the voltage of PIC terminals under nominal conditions, v^1 is the positive sequence voltage, v^2 is negative sequence voltage, and v^0 is the zero sequence voltage of PIC terminals. Finally, the reference currents in $\alpha\beta$ frame are calculated using Eq. (8):

$$\begin{bmatrix} i_\alpha^{ref} \\ i_\beta^{ref} \end{bmatrix} = \frac{1}{\left(v_\alpha^1\right)^2 + \left(v_\beta^1\right)^2} \begin{bmatrix} v_\alpha^1 & v_\beta^1 \\ v_\beta^1 & -v_\alpha^1 \end{bmatrix} \begin{bmatrix} P_{PIC} \\ Q_{PIC} \end{bmatrix} \tag{8}$$

A.2. Decreasing voltage unbalance index

If the load of AC sub-grid is unbalanced, it causes an unbalanced current flowing in the system, and as a result of unbalanced voltages in system impedances, the load voltage will be unbalanced, too. To compensate voltage unbalance, the PIC can be used as a current source [32]. If the distributed generation unit generates a balanced voltage in the AC sub-grid, Fig. 4 can be considered as a model of AC sub-grid and PIC. Assuming that injecting a current proportional to the zero and negative sequences of voltage into the AC sub-grid causes the voltage unbalance indices to decrease, the circuit equations of Fig. 4 are obtained as Eq. (9). In Fig. 4, k_0 and k_2 are the real or complex coefficients and v^0 and v^2 are the zero and negative sequence load voltages, respectively.

$$v_L^{012} = A^{-1} \frac{Z_{load} z_{ln}^{-1}}{M + Z_{load} z_{ln}^{-1}} A v_s^{012}; \quad v_s^{012} = \begin{bmatrix} 0 \\ V_s \\ 0 \end{bmatrix}$$
$$M = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} - \frac{k_0}{3} \begin{bmatrix} Z_{La} \\ Z_{Lb} \\ Z_{Lc} \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}^T - \frac{k_2}{3} \begin{bmatrix} Z_{La} \\ aZ_{Lb} \\ a^2 Z_{Lc} \end{bmatrix} \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix}^T \tag{9}$$

where, $Z_{load} = \begin{bmatrix} Z_{La} & 0 & 0 \\ 0 & Z_{Lb} & 0 \\ 0 & 0 & Z_{Lc} \end{bmatrix}$ $A = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}$

$a = 1\angle 120^\circ$

$$z_{ln} = \begin{bmatrix} z_{la} + z_n & z_n & z_n \\ z_n & z_{lb} + z_n & z_n \\ z_n & z_n & z_{lc} + z_n \end{bmatrix}.$$

By analyzing Eq. (9), it can be shown that by increasing k_0 and k_2 the zero and negative sequence voltages decrease (as shown in Fig. 5 and according to Table 1). Also, it can be shown that increasing the coefficients k_0 and k_2, respectively, does not significantly change the negative and zero sequence voltages. Therefore, it can be concluded that the compensation of the unbalanced indices is done in two separate channels. Although excessively increasing these coefficients causes the PIC current to increase and finally causes PIC to be overloaded. Therefore, the increase of these coefficients must be limited by another factor. This limitation is controlled by the current flowing through each leg and adjusting the value of unbalance compensation reference. Coefficients k_0 and k_2 are admittances that provide a path for the zero and negative sequence load current to flow. Since the load impedance is often resistive-inductive, by selecting a resistive-inductive admittance (the impedance of which will be resistive-capacitive), the current flowing through PIC can be decreased and consequently greater values can be selected for k_0 and k_2.

To calculate the values of k_0 and k_2, first different sequence components of the voltage of PIC terminals are separated from each other. Voltage unbalance indices of zero and negative sequence are calculated using Eq. (10):

$$UF_0 = \frac{v_{rms}^0}{v_{rms}^1} \quad UF_2 = \frac{v_{rms}^2}{v_{rms}^1} \tag{10}$$

The error between these values and their reference values passes through the PI controller and then, the values of k_0 and k_2, are obtained. The angles of coefficients k_0 and k_2 are created using a complex number $(1\angle\theta)$. Through multiplying these coefficients by zero and negative sequence voltages, i'_{abc} and i^0 , shown in Fig. 4, can be obtained. Adding up the current of power transferred between sub-grids and currents related to decreasing voltage unbalance generates the PIC reference current. Furthermore, the reference current of fourth leg of PIC

Table 1. Specifications of the hybrid AC-DC microgrid

Nominal voltage of DC sub-grid	220 V	Lines impedance	$z_{la} = 0.08 + 0.03j\Omega \quad z_{lb} = 0.05 + 0.095j\Omega$ $z_{lc} = 0.05 + 0.19j\Omega \quad z_n = 0.04 + 0.15j\Omega$
V_{DC}^{ref}	231 V	Output filter of SIC	$L_{Si} = 7mH \quad C_{Si} = 13.8\mu F \quad L_{sn} = 2mH$
R_d	0.0968 Ω	Series transformer	$S_n = 10kVA$ $Z_t = 0.03 + j0.1pu$ $n = 3$
P_{DC}^{max}	50 kW	SIC's controller parameters	$N = 1200 \quad K_f = 10 \quad k_{dpd} = 3 \times 10^{-4}$ $k_{ppd} = 8 \quad \omega_r = 10 \quad k_{ppr} = 3$ $k_{ipr} = 35$
C_f and C_B	4000 μF	PIC's controller parameters	$k_{ppr} = 1 \quad k_{ipr} = 4 \quad \omega_r = 6$ $k_{ppr0} = 2 \quad k_{ipr0} = 12 \quad \omega_{r0} = 6$ $\theta = 60°$
L_f	3 mH	Output filter of PIC	$L_{fi} = 6mH \quad L_{ni} = 3mH$
r_l	0.01 Ω	The load impedance related to Fig. 5	$Z_{La} = 500\Omega \quad Z_{Lb} = 3.25 + j2.2\Omega$ $Z_{Lc} = 1.55 + j1.2\Omega$

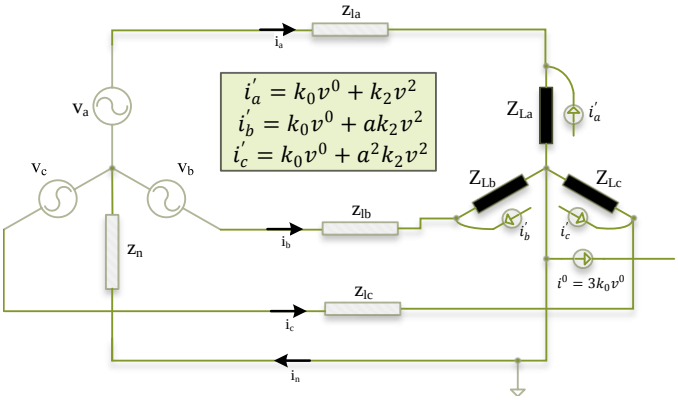

Fig. 4. Simplified model of the AC sub-grid and PIC.

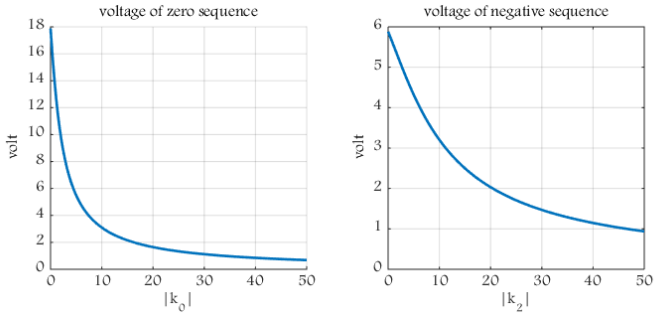

Fig. 5. The effect of k_0 and k_2 coefficients on reduction of zero and negative sequence voltages.

will be i^0. Fig. 6 shows the control system of PIC in the $\alpha\beta 0$ reference frame.

A.3. Determining the voltage unbalance compensation reference

As was explained before, PIC uses its free capacity to provide additional services such as compensating voltage unbalance. Therefore, for doing this the capacity of converter is always changing and these variations must be considered in the control system in order to avoid overloading PIC.

Basically in literature, the rated power of converters and the

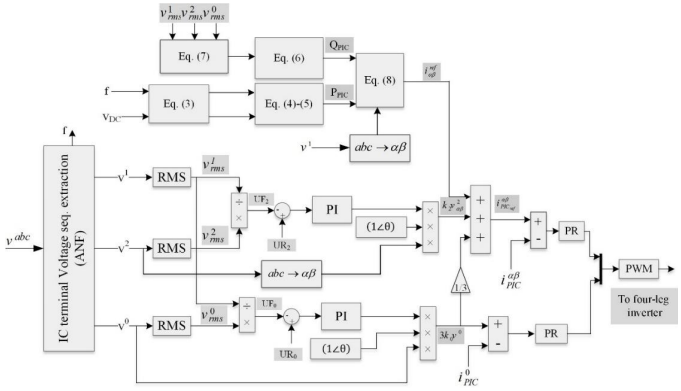

Fig. 6. The control system of PIC.

amount of injected power is used to calculate their free capacity. This is useful for converters which work under balanced conditions. In this paper, in order to prevent overloading PIC, the value of effective current of each leg is used for determining the compensation reference is used in a droop manner:

$$I_M = \max\left(i_a^{PIC-rms}, i_b^{PIC-rms}, i_c^{PIC-rms}, i_n^{PIC-rms}\right)$$
$$I_N = \max\left(i_a^{PIC-rms}, i_b^{PIC-rms}, i_c^{PIC-rms}\right) \quad (11)$$

$$UR_0 = UF_0 - m_0\left(I_R - I_M\right)$$
$$UR_2 = UF_2 - m_2\left(I_R - I_N\right) \quad (12)$$

where *max* is a function used for selecting the maximum value between inputs, m_0 and m_2 are the slopes of the droop curve of unbalance reference value, I_R is the maximum allowable value of the current of each leg, UR_0 and UR_2 are the compensation references of zero and negative sequence components of voltage. Eq. (12) causes the compensation reference to be determined in a floating manner therefore prevents overloading the converter.

B. The reference voltage of SIC

The reference voltage of SIC is obtained through extracting positive sequence component of PCC voltage. Various approaches have been proposed for doing this. In this paper, an adaptive

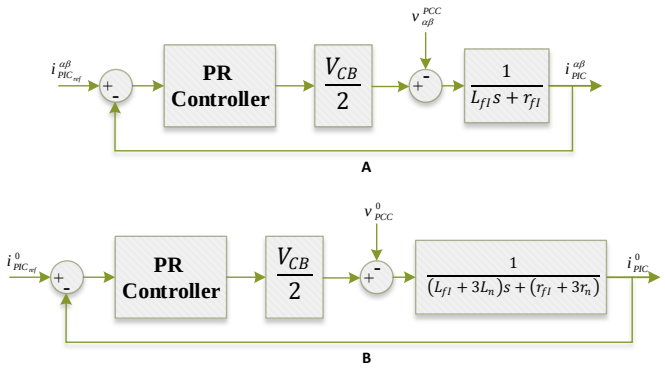

Fig. 7. Closed loop current control block diagram of 4-leg converter in $\alpha\beta 0$ frame.

notch filter is used to do so [33]. After extracting the positive sequence voltage, the value of its amplitude is used for detecting voltage sag. The amplitude of positive sequence is calculated using Eq. (13):

$$V_M = \sqrt{\left(v_a^1\right)^2 + \frac{\left(v_b^1 - v_c^1\right)^2}{3}} \tag{13}$$

4. MODELING AND CONTROLLER OF IC

As was explained before, by injecting/absorbing a current similar to reference current, the PIC causes the power to be exchanged between two sub-grids and voltage unbalance in the AC sub-grid side to decrease. This is done by generating a series of switching pulses by a controller with PWM technique. This is also the case in SIC. The only difference is that in SIC a voltage proportional to disturbances of PCC voltage will be injected into the sensitive load.

A. PIC converter

PIC is a 4-leg converter which in fact plays the role of a controlled current source. Closed loop current control of the 4-leg converter has been performed in [34] in $\alpha\beta 0$ frame. Fig. 7 shows this model along with current controller for PIC. This type of current controller is selected due to its ability to properly track the sinusoidal reference signal by a proportional-resonant controller. Eq. (14) represents the transfer function of this controller:

$$G_{PR}(s) = k_p + \frac{2k_i\omega_r s}{s^2 + 2\omega_r s + \omega_0^2} \tag{14}$$

where k_p, k_i, ω_r, and ω_0 are the proportional coefficient, integral coefficient, bandwidth, and resonance frequency of the controller, respectively. The way in which the coefficients of controller are determined has been fully described in [35].

B. The SIC converter

To model the SIC, governing equations the system shown in Fig. 8 are presented by Eqs. (15)-(19).

$$v_{SCk} = v_{CSk} + L_S\frac{di_{sk}}{dt} + L_n\frac{di_n}{dt}; \quad k = a,b,c \tag{15}$$

$$i_{sk} = i_{ck} + ni_{Lk}; \quad k = a,b,c \tag{16}$$

$$i_{ck} = C_S\frac{dv_{CSk}}{dt}; \quad k = a,b,c \tag{17}$$

$$v_{SICk} = n\left[v_{CSk} - ni_{Lk}Z_t\right]; \quad k = a,b,c \tag{18}$$

$$i_n = \sum_{k=a,b,c} i_{sk} \tag{19}$$

Using the Clarke Transformation (20), Eqs. (15)-(19) are transferred to the $\alpha\beta 0$ frame.

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{20}$$

$$\begin{bmatrix} v_{SC\alpha} \\ v_{SC\beta} \\ v_{SC0} \end{bmatrix} = \begin{bmatrix} v_{CS\alpha} \\ v_{CS\beta} \\ v_{CS0} \end{bmatrix} + L_S\begin{bmatrix} \frac{di_{s\alpha}}{dt} \\ \frac{di_{s\beta}}{dt} \\ \frac{di_{s0}}{dt} \end{bmatrix} + 3L_n\begin{bmatrix} 0 \\ 0 \\ \frac{di_{s0}}{dt} \end{bmatrix} \tag{21}$$

$$\begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \\ i_{s0} \end{bmatrix} = \begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \\ i_{c0} \end{bmatrix} + n\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix} \tag{22}$$

$$\begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \\ i_{c0} \end{bmatrix} = C_S\begin{bmatrix} \frac{dv_{CS\alpha}}{dt} \\ \frac{dv_{CS\beta}}{dt} \\ \frac{dv_{CS0}}{dt} \end{bmatrix} \tag{23}$$

$$\begin{bmatrix} v_{SIC_\alpha} \\ v_{SIC\beta} \\ v_{SIC0} \end{bmatrix} = n\left(\begin{bmatrix} v_{CS\alpha} \\ v_{CS\beta} \\ v_{CS0} \end{bmatrix} - nZ_t\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix}\right) \tag{24}$$

Using these equations, the model of power stage of SIC in the $\alpha\beta 0$ stationary frame is depicted in Fig. 8. Two controllers are used in the control section of each phase. The PR controller, which guarantees that the erorr between the output and reference voltages is zero, generates the reference current of the output capacitor (C_S). As it clear from Eq. (24), the SIC output voltage is a function of the voltage of C_S. On the other hand, the variation rate of the capacitor voltage is proportional to its current. Therefore, the output voltage of SIC can be controlled by controlling the capacitor current. Consequently, by feeding back the current and making it pass through a proportional gain block which plays the role of a virtual resistance (virtual impedance improves system stability), the error between the reference and capacitor currents is calculated. A controller of PD type is selected as the capacitor current controller. The features of PD controller include increasing transient response speed, improving the system bandwidth, and finally improving stability. The transfer function of this controller is as presented by Eq. (25):

$$G_{PD}(s) = k_p + k_d\frac{N \times s}{N + s} \tag{25}$$

where k_p is the proportional gain, k_d is the differential gain, and N is a large number. According to Fig. 9, the load voltage in $\alpha\beta 0$ frame is:

$$\begin{aligned} v_L^{\alpha\beta} &= G_S v_{ref}^{\alpha\beta} + G_D v_{pcc}^{\alpha\beta} \\ v_L^0 &= G_Z v_{ref}^0 + G_X v_{pcc}^0 \end{aligned} \tag{26}$$

The transfer function of G_S, G_D, G_Z, and G_X shows in Eqs. (27)-(30) and the frequency response of this equations, considering the specifications presented in Table 1, are shown in Fig.

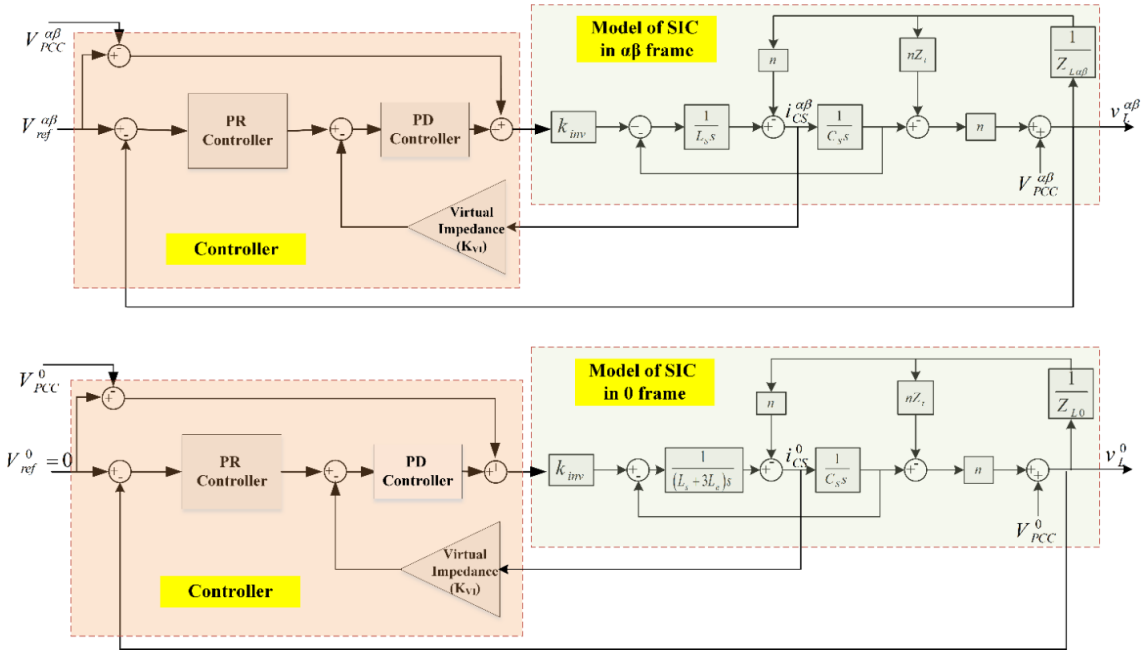

Fig. 9. Block diagram of closed loop system control of SIC in $\alpha\beta 0$ frame.

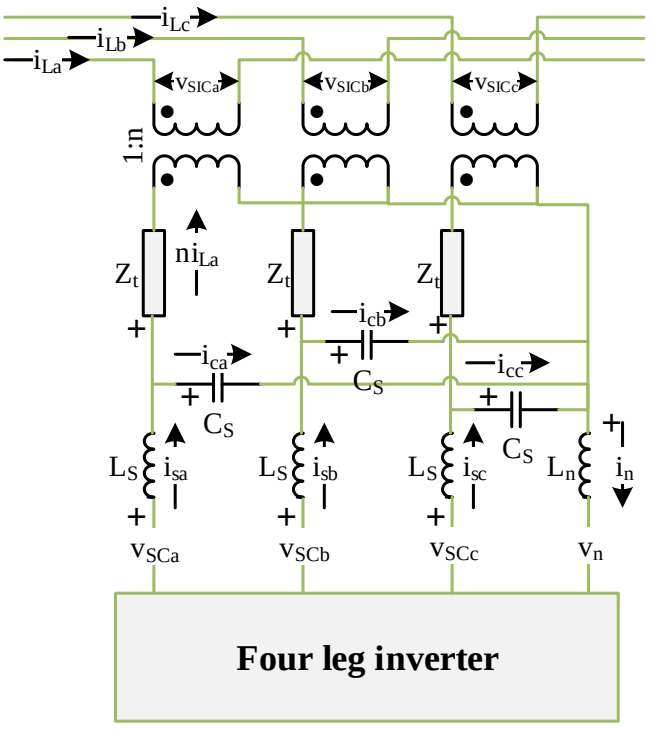

Fig. 8. SIC converter structure.

10. It is clear from the frequency response of the system that the output voltage is slightly affected by PCC voltage (red line in Fig. 10) and properly tracks the reference voltage (blue line in Fig. 10) because of the wide bandwidth. Also, the wide bandwidth makes the control system response very fast in following the reference voltage signal. Therefore, the load voltage will be equal to the reference voltage signal corresponding to the positive sequence voltage of the fundamental component.

It should be noted that the reference voltage signal of the zero se-quence is equal to zero, so the sensitive load voltage will be perfectly symmetrical.

5. SIMULATION RESULTS

In this section, simulation results of the system shown in Fig. 2 under different scenarios are presented. There is a power generation unit in the both AC and DC sub-grids. The impedances of distribution lines in AC sub-grid are considered to be unbalanced so that the system performance can be tested under more difficult conditions. All the loads connected to the AC sub-grid are considered to be resistive-inductive loads with a power factor of 0.8. The method of determining the size of passive ele-ments is described in [37]. Simulations are carried out in MATLAB/SIMULINK environment. System specifications and the values of controller parameters are presented in Table 1.

It is worth mentioning that the PI controllers in Fig. 6 are tuned through the second method of Ziegler and Nichols [36]. The PR control-ler in the PIC is set according to the method presented in [35]. Also, the PD and PR controllers are tuning in SIC by using the Genetic Optimiza-tion algorithm and defining constrains 60-degree phase margins, gain margins greater than 6 dB and settling times less than 2 milliseconds.

A. The first scenario

In the first scenario, two 8.5 kW single phase loads are placed at lines b and c, and a 1.5 kW load is placed at the sensitive load bus. The DC sub-grid load is considered to be 45 kW. At t=0.8 sec, the PIC enters the system and transfers the power from the AC sub-grid to the DC sub-grid.

The result of this, as can be seen in Fig. 11, is an increase in the voltage of DC sub-grid. Under these conditions, the load of the AC sub-grid is unbalanced and PIC is responsible for de-

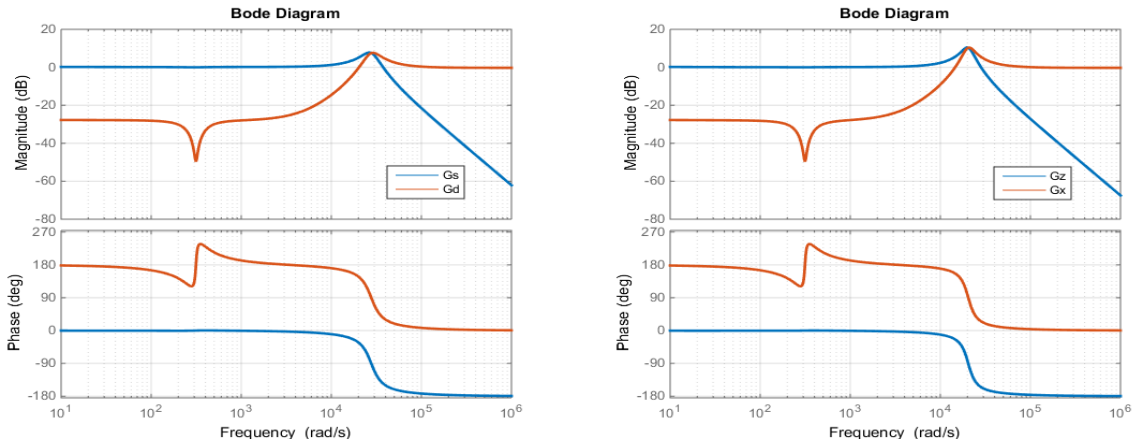

Fig. 10. The frequency response of Eqs. (27)-(30).

creasing the voltage unbalance indices. The voltage unbalance compensator is activated at t=1.2 sec. Therefore, current of PIC becomes unbalanced and decreases the voltage unbalance indices in proportion to the free capacity of PIC. With regard to the current of PIC shown in Fig. 11, after activation of the compensating section (t=1.2 sec), the current of legs 'a' and 'n' increase and the current of legs 'b' and 'c' decrease. These changes can be attributed to the ways the loads are placed in the network. The SIC which is placed between the sensitive load and PCC provides a balanced voltage for the sensitive load. The SIC has entered the system at t=1.5 sec. The SIC reference voltage is in accordance with the positive sequence voltage of the fundamental component. Therefore, the SIC adds any perturbation that is different from the reference voltage to the voltage of sensitive load. A summary of the system state is presented in Table 2.

Table 2. A summary of the state of microgrid in the first scenario

	IC disable	IC enable
Voltage of DC sub-grid	205 V	212 V
Frequency of AC sub-grid	50.2 Hz	49.8 Hz
Power transferred between 2 sub-grids	0	12 kW
Voltage unbalance index	UF_0=0.04	UF_0=0.03
	UF_2=0.018	UF_2=0.016
Voltage of sensitive load	V_a=221 V	V_a=218 V
	V_b=214 V	V_b=218 V
	V_c=216 V	V_c=217 V

B. The second scenario

In the second scenario, three unbalanced load and a sensitive load are connected to the AC sub-grid. These loads consume a total power of 39 kW. The load of the DC sub-grid is equal to 10 kW. Therefore, the PIC transfers the power from the DC sub-grid to the AC sub-grid. The activation times of the different parts of the system are the same as the first scenario. The results of this simulation are shown in Fig. 12. It can be seen from Fig. 12 that the power transferred from the DC sub-grid to the AC sub-grid causes the voltage of the DC sub-grid to drop. The zero sequence voltage unbalance factor also decreased from 4% to 2.5%. The current of leg 'n' in the PIC has reached to its maximum value so that no further decrease in the zero sequence unbalance factor is possible. However, the, negative sequence voltage unbalance factor is still decreasing and therefore increasing the current of legs 'abc'. Sensitive load voltage is balanced as previous scenario after SIC activation.

C. The third scenario

In the third scenario, the system performance against voltage sag is investigated. The power consumption of the DC sub-grid is equal to 45 kW and the power consumption of the AC sub-grid is unbalanced and equal to 21 kW. At t=2 sec, a 10 kW induction motor enters the system and causes a sag in the PCC voltage. It can be seen from Fig. 13 that the PCC voltage for 2 cycles is 200v. This voltage sag is unacceptable for sensitive load. Therefore, SIC compensates this disturbance for sensitive load. As can be seen in Fig. 13, the SIC protects the sensitive load voltage against voltage sag. For better visibility of SIC performance, the voltage sag moment is zoomed. The PIC also performs two tasks of power transfer (from DC sub-grid to AC sub-grid) and reduction of voltage unbalance factors.

6. CONCLUSIONS

In this paper, the structure of IC in the AC sub-grid was changed in order to improve voltage quality. Due to the proper performance of the 4-leg converters regarding the zero sequence component, this structure was used in the power stage of the IC. Simulation results show that this structure is capable of decreasing the voltage unbalance indices in the AC sub-grid at any moment in proportion to its free capacity. The free capacity of PIC varies in an adaptive way in accordance with the current flowing through each leg. Therefore, this approach prevents overloading PIC. The SIC converter provides a high-quality voltage for the sensitive load. An output capacitor current control and a virtual resistor are used in the control system of this converter. Therefore, the response of this system to the PCC voltage disturbances is very fast.

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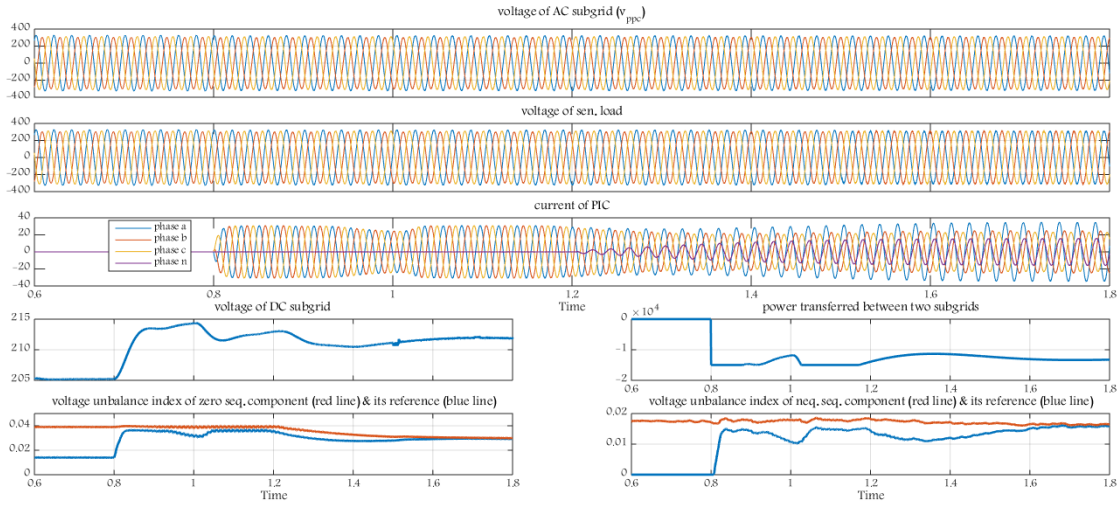

Fig. 11. Simulation results of the first scenario.

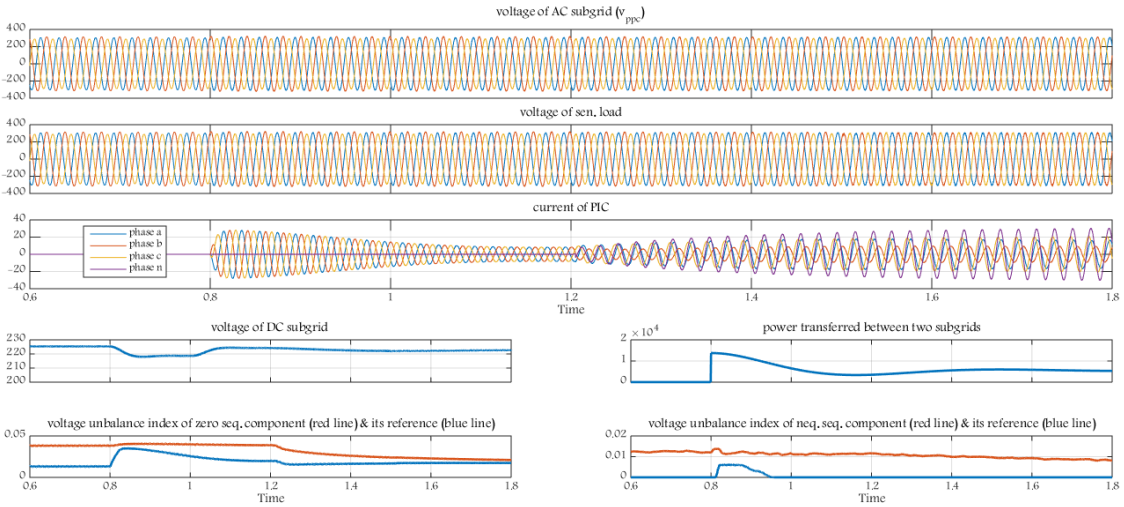

Fig. 12. Simulation results of the second scenario.

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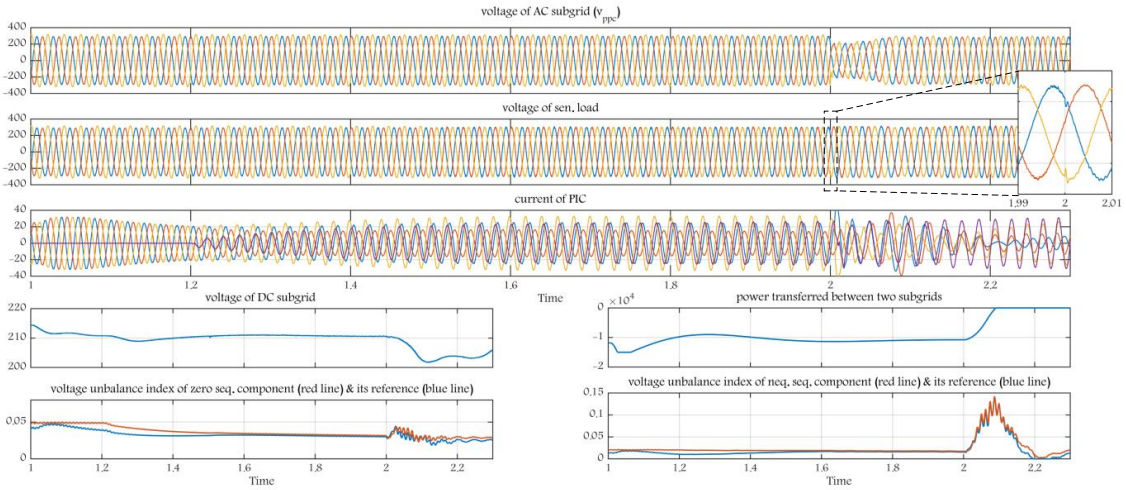

Fig. 13. Simulation results of the third scenario.

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$$G_S = \frac{Z_{L\alpha\beta} k_{inv} n \left(1 + G_{PD} G_{PR}\right)}{\left(C_S L_S Z_t n^2 + C_S L_S Z_{L\alpha\beta}\right) s^2 + \left(L_S n^2 + C_S Z_{L\alpha\beta} k_{inv} K_{VI} G_{PD} + C_S Z_t k_{inv} K_{VI} n^2 G_{PD}\right) s + \left(Z_t n^2 + Z_{L\alpha\beta} k_{inv} n G_{PD} G_{PR} + Z_{L\alpha\beta}\right)} \quad \textbf{(27)}$$

$$G_D = \frac{C_S L_S Z_{L\alpha\beta} s^2 - Z_{L\alpha\beta} k_{inv} n}{\left(C_S L_S Z_t n^2 + C_S L_S Z_{L\alpha\beta}\right) s^2 + \left(L_S n^2 + C_S Z_{L\alpha\beta} k_{inv} K_{VI} G_{PD} + C_S Z_t k_{inv} K_{VI} n^2 G_{PD}\right) s + \left(Z_t n^2 + Z_{L\alpha\beta} k_{inv} n G_{PD} G_{PR} + Z_{L\alpha\beta}\right)} \quad \textbf{(28)}$$

$$G_Z = \frac{Z_{L0} k_{inv} n \left(1 + G_{PD} G_{PR}\right)}{\left(C_S \left(L_S + 3L_n\right) Z_t n^2 + C_S \left(L_S + 3L_n\right) Z_{L0}\right) s^2 + \left(\left(L_S + 3L_n\right) n^2 + C_S Z_{L0} k_{inv} K_{VI} G_{PD} + C_S Z_t k_{inv} K_{VI} n^2 G_{PD}\right) s + \left(Z_t n^2 + Z_{L0} k_{inv} n G_{PD} G_{PR} + Z_{L0}\right)} \quad \textbf{(29)}$$

$$G_X = \frac{C_S \left(L_S + 3L_n\right) Z_{L0} s^2 - Z_{L0} k_{inv} n}{\left(C_S \left(L_S + 3L_n\right) Z_t n^2 + C_S \left(L_S + 3L_n\right) Z_{L0}\right) s^2 + \left(\left(L_S + 3L_n\right) n^2 + C_S Z_{L0} k_{inv} K_{VI} G_{PD} + C_S Z_t k_{inv} K_{VI} n^2 G_{PD}\right) s + \left(Z_t n^2 + Z_{L0} k_{inv} n G_{PD} G_{PR} + Z_{L0}\right)} \quad \textbf{(30)}$$